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Aims and Scope

The International Journal of Advances in Telecommunications, Electronics, Signals and Systems (IJATES²) is an all-electronic international scientific journal with the aim to bring the most recent and unpublished research and development results in the area of electronics to the scientific and technical societies, and is supported by the ISES (International Science and Engineering Society, o.s.). The journal's scope covers all the aspects of telecommunication, signal processing, theory and design of circuits and systems for electronics.

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Behavioral modeling of Digitally Adjustable Current Amplifier

J. Polak, L. Langhammer, and J. Jerabek

***Abstract*— This article presents the digitally adjustable current amplifier (DACA) and its analog behavioral model (ABM), which is suitable for both ideal and advanced analyses of the function block using DACA as active element. There are four levels of this model, each being suitable for simulation of a certain degree of electronic circuits design (e.g. filters, oscillators, generators). Each model is presented through a schematic wiring in the simulation program OrCAD, including a description of equations representing specific functions in the given level of the simulation model. The design of individual levels is always verified using PSpice simulations. The ABM model has been developed based on practically measured values of a number of DACA amplifier samples. The simulation results for proposed levels of the ABM model are shown and compared with the results of the real measurements of the active element DACA.**

***Keywords*—Digitally adjustable current amplifier, controllable gain, DACA, ABM model, PSpice, modeling.**

I. Introduction

Many scientific articles in professional journals describe the design of frequency filters with a clear objective to create a universal filter e.g. with the lowest possible power consumption requirements. Those articles often focus on the design of filters working in the current mode (CM), with current considered as the input and output variable. The second option for the filter design is using the voltage-mode (VM) approach, with voltage considered as the input and output variable. These two modes can also be combined. When designing frequency filters, we have available active elements and their various modifications working on different principles, such as operational amplifiers (OPA), operational transconductance amplifiers (OTA), voltage conveyors (VC), current conveyors (CC), current feedback amplifiers (CFA), voltage followers (VF), current followers (CF), etc. [1]

An important parameter in the selection of an active element is the possibility of electronic control of the specific parameter (gain, input impedance, etc.) by means of DC current or DC voltage. Controllable active element consists of simpler uncontrollable and controllable active elements. One of the fundamental active elements is the current differencing buffered amplifier (CDBA) [2], which can be created from two active elements current feedback amplifier (CFA) [2], [3], implemented for example through AD844 [4], [5].

By replacing the voltage buffer in the active element CDBA by an balanced-output operational transconductance amplifier (BOTA), an active element CDTA [6], [7] is created. The function of this circuit shows that it is possible to regulate the gain using transconductance and that it is suitable for use in construction of filters working in the current mode [6]. The current follower transconductance amplifier (CFTA) [8], with only one current input, is based on a similar principle as CDTA. CFTA transconductance is controllable and it is suitable for the construction of filters in the current mode.

Other parameters of active elements are often also electronically controlled, usually using DC current. The active element current-controlled current conveyor transconductance amplifier (CCCCTA) [9] is based on the principle of current conveyor transconductance amplifier (CCTA) presented in [10], but there is a controllable input impedance at input x, which can be controlled by current, as shown in [9]. CCCCTA may be created using a current controlled current conveyor (CCCII) [11] and OTA. By combination of these active elements, we can also create a current controlled current follower transconductance amplifier (CCCFTA) [12]. In that case the input y of CCCII is grounded and the OTA replaced by a BOTA. This active element is again electronically controllable through current as for CCCCTA.

Another group of controllable active elements are the digitally controlled active elements. Their properties are controlled by digital *n*-bit word. One of the digitally controlled active elements is the digitally controlled current conveyor (DCCC) [13]. This element is digitally controlled using current division network (CDN) [13], wherein the number of control bits is determined by the number of current division cells (CDC) [13]. Another possibility of creating CDC is based on the use of the unity-gain current amplifier with very low-resistance input terminal [14] and a current divider circuit. This principle is the basis for the digital control of the element digitally controlled current follower (DC-CF) [15].

The active element controlled using the digital word, presented in this article, is the digitally adjustable current amplifier (DACA) [16], [17]. It has been recently developed by the Department of Telecommunications of the Brno

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University of Technology in cooperation with the company ON Semiconductor, based on verified technology in CMOS 0.35 µm, suitable for analogue signal processing. The active element DACA can be used for instance in circuits of frequency filters, oscillators and function generators [18]-[21]. In this paper we present newly designed ABM models [22] of the element DACA in four levels (zero, first, second, third level) in PSpice. As it is discussed in section III, the zero model describes only basic (ideal) behavior of the DACA. The first model is designed so that it reflects the inputs and outputs resistances and real values of gain, the second model is similar to the first level and it is supplemented by other functions to show the frequency dependence of input and output impedance values for different gains. The third level takes into account the real current limits of the inputs and outputs. This is particularly suitable when simulating complex electronic circuits containing different types of elements, sub-circuits and devices, require different levels of modelling for different circuits and therefore make it impractical to include all the functions into a single level of simulation model [23]. Dividing the model into multiple levels, a more detailed examination of the desired characteristics of the analysed circuit can be provided.

II. FUNCTIONAL PRINCIPLES OF DACA

The active element DACA (Fig. 1a) consists of differential current inputs and outputs. Inputs are of low impedance and outputs high impedance characters. The current gain can be adjusted with unity step from 1 to 8 of the input current in the non-differential connection. In the differential connection, the gain can be adjusted with 2-unit step from 2 to 16 of the input current. The gain control is realized using a 3-bit bus (referred as CTR in Fig. 1a, b). The schematic symbol of the active element DACA is shown in Fig. 1a.

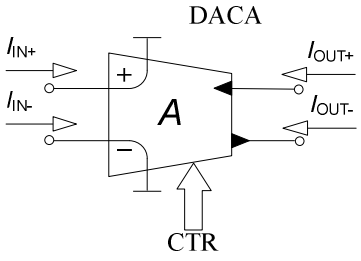

Fig. 1a. Schematic symbol of DACA element

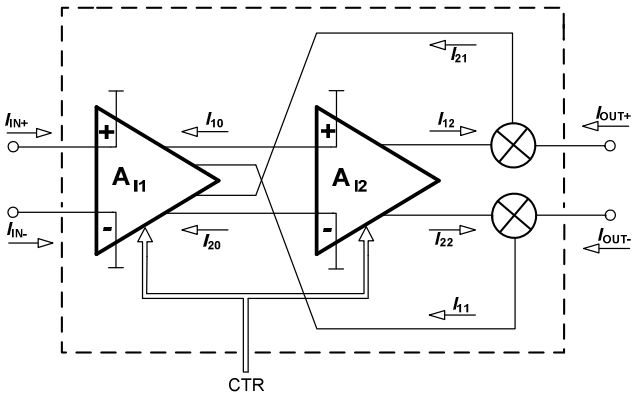

Fig. 1b. Block internal structure of DACA element

Figure 1b shows the internal structure of the circuit. It is based on a pair of digitally controlled current amplifiers. The relationship between internal and external currents is expressed by following equations:

$$I_{10} = I_{IN+}\,, \quad (1) \qquad I_{20} = I_{IN-}\,, \quad (4)$$

$$I_{11} = A_{I1} I_{IN+}\,, \quad (2) \qquad I_{21} = A_{I1} I_{IN-}\,, \quad (5)$$

$$I_{12} = A_{I2} I_{10}, \quad (3) \qquad I_{22} = A_{I2} I_{20}\,. \quad (6)$$

The resulting function of the circuit can be summarized as follows:

$$I_{DIF\_IN} = (I_{IN+} - I_{IN-}), \quad (7)$$

$$I_{DIF\_OUT} = (I_{OUT+} - I_{OUT-}), \quad (8)$$

$$I_{OUT+} = A_I (I_{IN+} - I_{IN-}), \quad (9)$$

$$I_{OUT-} = -A_I (I_{IN+} - I_{IN-}), \quad (10)$$

$$I_{DIF\_OUT} = 2A_I I_{DIF\_IN}, \quad (11)$$

with A_I as the current gain of the active element DACA and $I_{\mathrm{DIF\_IN}}$, $I_{\mathrm{DIF\_OUT}}$ as the input and output differential currents.

III. ABM MODEL OF DACA

The ABM model for the active element DACA was developed to create the best approximation of circuit characteristics considered in the simulations during the design of electrical circuits that use this active element. The ABM model consists of several levels, each level adds certain undesired, but realistic, characteristics (e.g. input impedance, output impedance, frequency dependence, DC limitations) corresponding to the real properties of the DACA element. The use of individual levels in the model design allows us to identify and analyse how the adverse effects influence the function of the circuit.

A. Zero level macro model

The zero level of the model represented in Fig. 2 is designed so that the element behaves as ideal. The use of the active element is not affected by any adverse effects. Parts labelled F1-F4 represent current-controlled current sources and their task is to simulate ideal transmissions of the controllable current amplifier DACA using specified functions. The following equations show the internal current source F3 function, equation (12), into which are substituted values from equation (14) following the variation of the input variable *gain*. The current source F4 is represented by equation (13), into which are substituted values from equation (15), again depending on the variation of *gain*. Equations (12-15) are control functions directly used for the PSpice simulation program.

$$\mathrm{GAIN} = \{\mathrm{F3@funcref(@gain)}\}, \quad (12)$$

$$\mathrm{GAIN} = \{\mathrm{F4@funcref(@gain)}\}, \quad (13)$$

$$.FUNC\ \mathrm{F3@funcref(g)} = \{\mathrm{TABLE\ (g,1,1,2,2,3,3,4,4,5,5,6,6,7,7,8,8)}\}, \quad (14)$$

$$.\mathrm{FUNC\ F4@funcref(g)} = \{\mathrm{TABLE\ (g,1,-1,2,-2,3,-3,4,-4,5,-5,6,-6,7,-7,8,-8)}\}. \quad (15)$$

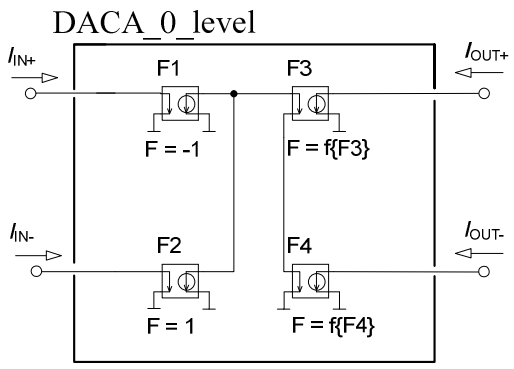

Fig. 2. Model of the zero level of DACA element

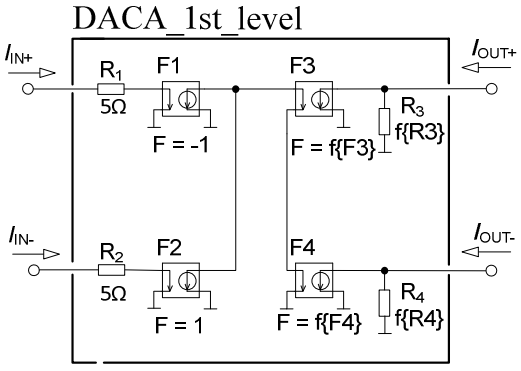

Fig. 3. Model of the first level of DACA element

B. *First level macro model*

The first level of the DACA simulation model (Fig. 3) is designed so that it reflects the inputs and outputs resistances and real values of gain. Input resistance (resistors R_1 and R_2) is the same for all values of gain. The values of the output resistances (resistors R_3 and R_4) are chosen depending on the selected value *gain*. The gain of components F3 and F4 already corresponds to the real measured gain values of the element DACA. Into equations (12) and (13) are substituted values from equations (18) and (19). For resistors R_3 and R_4 the value of resistance (variable *IMP1*) changes with the variation of gain according to equations (16) and (17), which results in variation in the output impedance depending on the selected gain. The resistor R_3 is represented by equation (16), into which are substituted values from equation (20). Similarly, resistor R_4 is represented by equation (17), into which are substituted values from equation (21), in both cases depending on the value of specific gain.

$$IMP1 = \{Fr3@funcref(@gain)\}, \quad (16)$$

$$IMP1 = \{Fr4@funcref(@gain)\}, \quad (17)$$

$$.FUNC\ F3@funcref(g) = \{TABLE\ (g, 1{,}0.779, 2{,}1.594, 3{,}2.489, 4{,}3.299, 5{,}4.133, 6{,}4.936, 7{,}5.814, 8{,}6.609)\}, \quad (18)$$

$$.FUNC\ F4@funcref(g) = \{TABLE\ (g, 1{,}-0.801, 2{,}-1.633, 3{,}-2.55, 4{,}-3.378, 5{,}-4.232, 6{,}-5.054, 7{,}-5.951, 8{,}-6.763)\}, \quad (19)$$

$$.FUNC\ Fr3@funcref(g) = \{TABLE\ (g, 1{,}72762.57, 2{,}34139.24, 3{,}21155.61, 4{,}15713.62, 5{,}11815.86, 6{,}9862.1, 7{,}8323.96, 8{,}7236.25)\}, \quad (20)$$

$$.FUNC\ Fr4@funcref(g) = \{TABLE\ (g, 1{,}72748.87, 2{,}34119.5, 3{,}21390.12, 4{,}15890.39, 5{,}12044.26, 6{,}10046.73, 7{,}8430.3, 8{,}7335.59)\}. \quad (21)$$

Equations (18) and (19) show that at higher gain values the output current values differ more significantly from the ideal current values specified in equations (14) and (15). Increasing the *gain* value also reduces the value of the output impedance. This statement is supported by the output resistance values specified in equations (20) and (21) for both outputs depending on the *gain*. The value of the output impedance is the highest at gain equal to 1, approximately 72 kΩ.

C. *Second level macro model*

The design of the second level of the simulation model presented in Fig. 4 is similar to the first level and is completed by other functions to show the frequency dependence of input and output impedance values for different gains. The frequency dependence is simulated using capacitors C_3 and C_4, whose functions are given in equations (22) and (23). These equations are then supplemented by values from equations (24) and (25) depending on selected *gain* level.

$$\text{F\_formula} = \{FC3@funcref(@gain)\}, \quad (22)$$

$$\text{F\_formula} = \{FC4@funcref(@gain)\}, \quad (23)$$

$$.FUNC\ FC3@funcref(g) = \{TABLE\ (g, 1{,}12.2p, 2{,}12.6p, 3{,}12.7p, 4{,}12.9p, 5{,}13.4p, 6{,}13.6p, 7{,}13.6p, 8{,}13.4p)\}, \quad (24)$$

$$.FUNC\ FC4@funcref(g) = \{TABLE\ (g, 1{,}12.5p, 2{,}12.4p, 3{,}13.1p, 4{,}13.3p, 5{,}13.7p, 6{,}13.9p, 7{,}13.7p, 8{,}13.5p)\}. \quad (25)$$

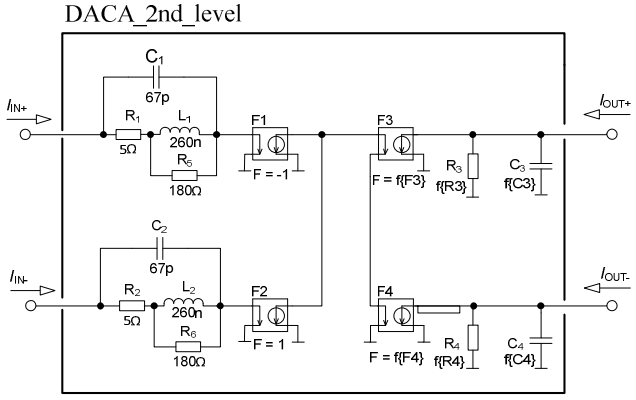

Fig. 4. Model of the second level of DACA element

As an example, Fig. 5 shows the frequency dependence of the output current at output OUT+ for the different gain levels. The results shown in the graph were obtained by excitation of input IN+ by input current I_{IN+} = *1* mA with connected load 50 Ω on OUT+. Approximately until reaching the frequency of 10 MHz, the output current at output OUT+ (Fig. 5) and OUT- (similar results to OUT+) are constant. At higher frequencies, there is a decrease in the ability of the amplifying gain values, reflected in a decrease of both output currents (OUT+ and OUT-).

Similar frequency dependence can be seen in the graph in Fig. 6, showing the frequency dependence of the output impedance for output OUT+. The decrease in the output impedance starts at *gain* value equal to 1 already at a frequency of 15 kHz, whereas at *gain* value equal to 8 it only starts at a frequency of 500 kHz.

Fig. 7 shows the frequency dependence of the input impedance. The input impedance of the amplifier is constant Z_{IN} = *5* Ω for all values of *gain* and its frequency dependence is reflected in slight growth from 1 MHz and then a steep increase from 10 MHz.

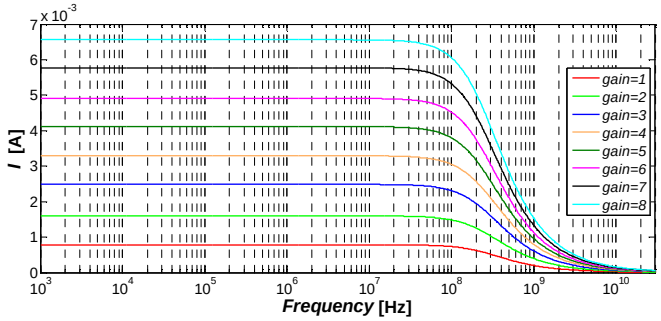

Fig. 5. Output current I_{OUT+} for each value of gain

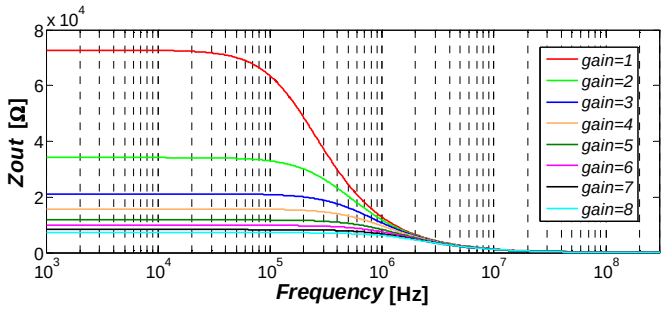

Fig. 6. Output impedance Z_{OUT+} for each value of gain

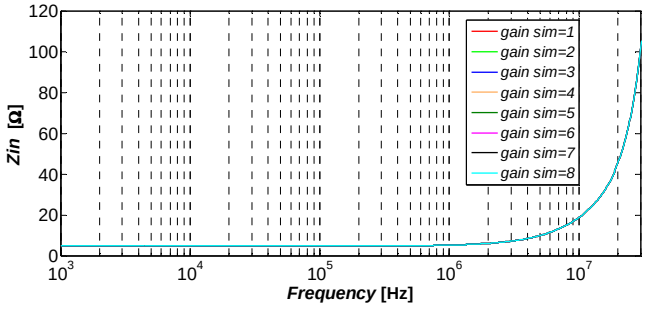

Fig. 7. Input impedance Z_{IN+} for each value of gain

D. Third level macro model

The third level of the simulation model represented in Fig. 8 takes into account the real current limits of inputs and outputs. Input current limit is defined by inserting the function represented by equation (26) into the element F1 and the equation (27) into the element F2 of the proposed model. Upper and lower input current limit is fixed by using variables *HI(High)* = *300* µA *and LO(Low)* = *-300* µA. The output current limit is realized by inserting function (26) into elements F5 and F6. Values of variables HI and LO from equations (28) and (29) are then substituted into equation (26). Subsequently, in equation (28) values are added depending on the currently selected gain (variable *gain*) from equation (31), which sets the current limit of element F5. To set the element F6 we use equation (26) and add to it the values of current HI and LO from equations (30) and (29). Then we assign values to load depending on the currently selected *gain* from equation (32), which sets the current limit of element F6.

$$\text{F\_formula} = -LIMIT(@lin, @LO, @HI), \tag{26}$$

$$\text{F\_formula} = LIMIT(@lin, @LO, @HI), \tag{27}$$

$$HI = F5@funcref(@gain), \tag{28}$$

$$LO = -@HI, \tag{29}$$

$$HI = F6@funcref(@gain), \tag{30}$$

$$\begin{aligned}&\text{. FUNC F5@funcref(g)}\\&= \{\text{TABLE (g, 1,300µ, 2,250µ, 3,200µ, 4,150µ,}\\&\text{5,100µ, 6,75µ, 7,50µ, 8,30µ)}\},\end{aligned} \tag{31}$$

$$\begin{aligned}&\text{. FUNC F6@funcref(g)}\\&= \{\text{TABLE (g, 1,300µ, 2,250µ, 3,200µ, 4,150µ,}\\&\text{5,100µ, 6,75µ, 7,50µ, 8,30µ)}\}.\end{aligned} \tag{32}$$

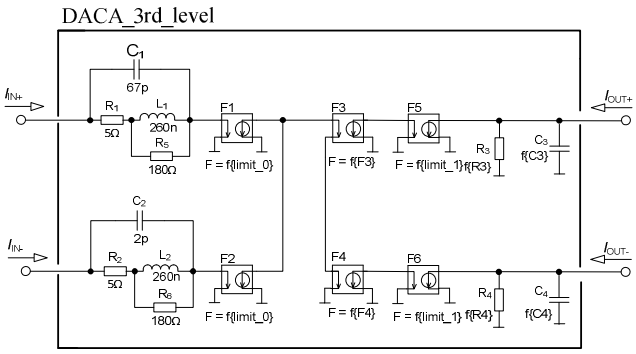

Fig. 8. Model of the third level of DACA element

The functions of the input and output current limit are demonstrated in the graph in Fig. 9. The input current, connected to IN−, is the harmonic signal, which is indicated in the graph as I_{IN} and has the following parameters: amplitude 1 mA (intentionally too high for DACA element in order to show the limitations), frequency of 1 kHz. Gain of DACA is set to *gain* = 2. Input current after the limit element is represented by the curve marked as LIMIT I_{IN}. The amplitude of this curve is limited to 300 µA, according to the set values of upper and lower input current limit. Curves I_{OUT+} and I_{OUT-} represent output currents of the active element, their amplitude is limited to 250 µA and corresponds to the values of equations (31) and (32) for the current limit *gain* value equal to two. Furthermore, the graph in Fig. 9 shows the particular gain limit represented as GAIN LIMIT I_{IN} (gain is 2 in this particular case). This curve is based on the gain parameter defined in equation (18) for a gain value (variable *gain*) equal to two and the input current limit of element F1.

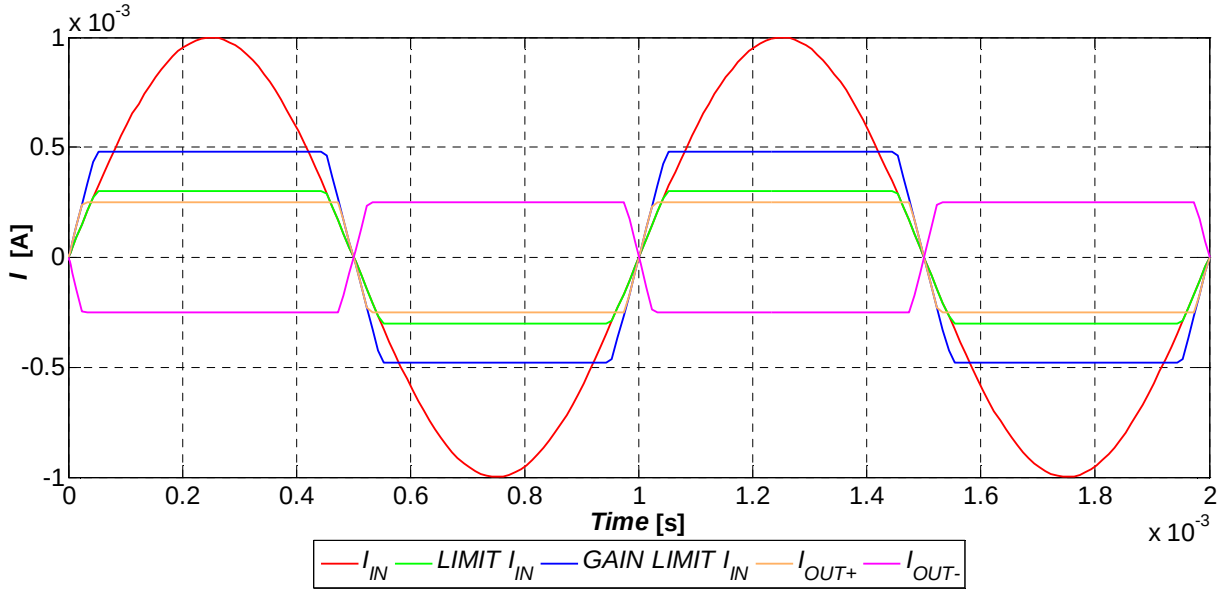

Fig. 9. Demonstration of current limitations in the third level of model in time domain

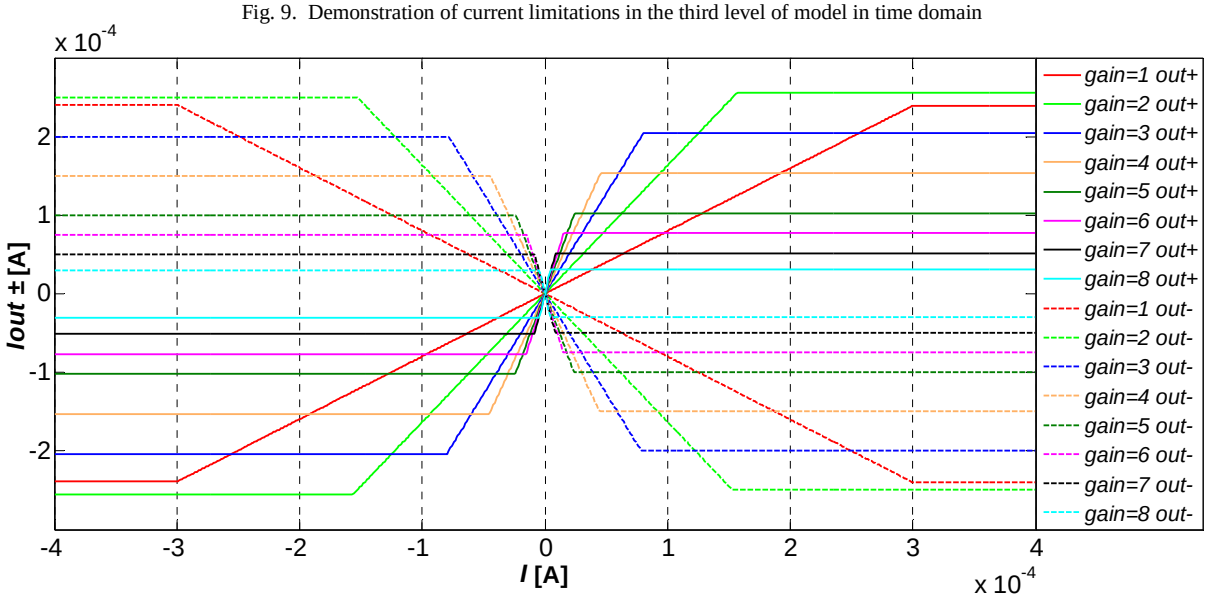

Fig. 10. Demonstration of current limitation for each value of gain in DC/DC graph

Fig. 10 shows the DC characteristics of the input current I_{IN}, connected to input I_{IN-} within the range −400 µA to +400 µA. The output currents for both outputs OUT+ and OUT− show the characteristic tendency for specific gain and for each gain value the current limit of elements F5 and F6 is reflected, according to equations (26) and (27). Minor deviations of the inverting and non-inverting output correspond to the behaviour of these outputs in a real active element DACA. The graph further clearly indicates that the current limit decreases with increasing gain.

IV. Comparison with Results from Practical Measurement

Numerical values presented in the ABM model were obtained through thorough measurements and subsequent analysis of the results of DC, AC, and impedance characteristics for eight of produced DACA chips [17]. Figure 11 shows the curves for all eight values of gain depending on frequency for both measurement and simulation model results (real DACA and ABM simulation model of DACA). When comparing curves in case of the graph in Fig. 11, there are some deviations of the ABM model from real element at higher gain values. The graph in Fig. 12 shows the frequency dependence of the output impedance for all eight values of gain again for ABM simulation model and real DACA element. When comparing curves in Fig. 12, we can observe nearly identical curves for the output impedance for the model DACA and the real element DACA. In the graph in Fig. 13 the input impedance corresponds to value Z_{IN} = 5Ω up to 1 MHz, for the model DACA and the real element DACA.

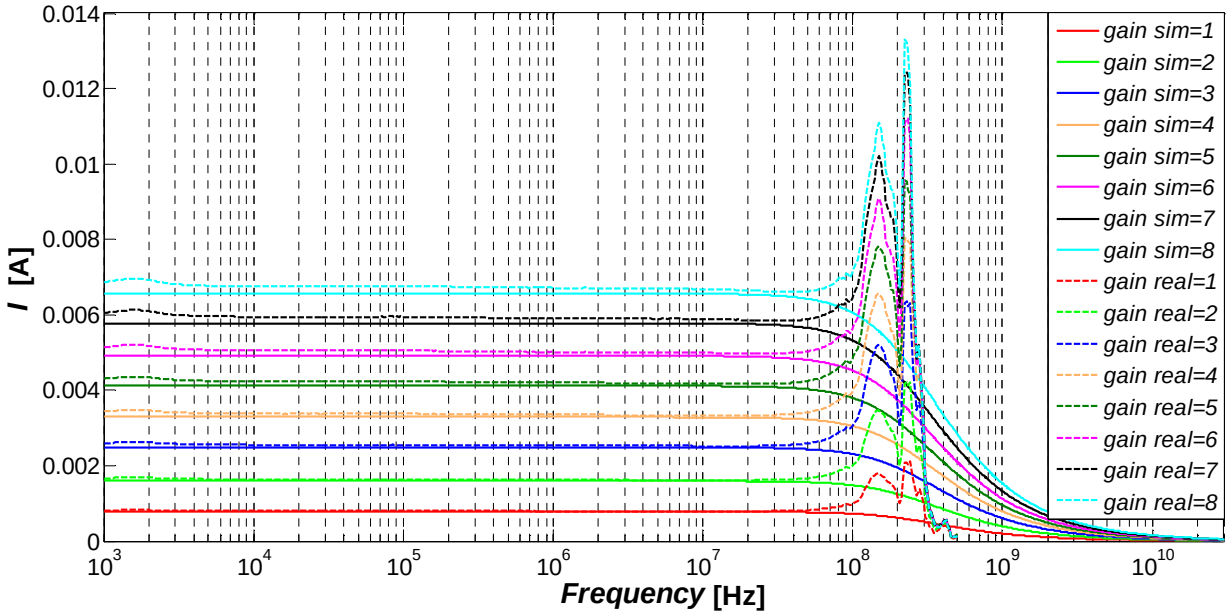

Fig. 11. Comparison of measured and simulated gain for all variants of gain in DACA

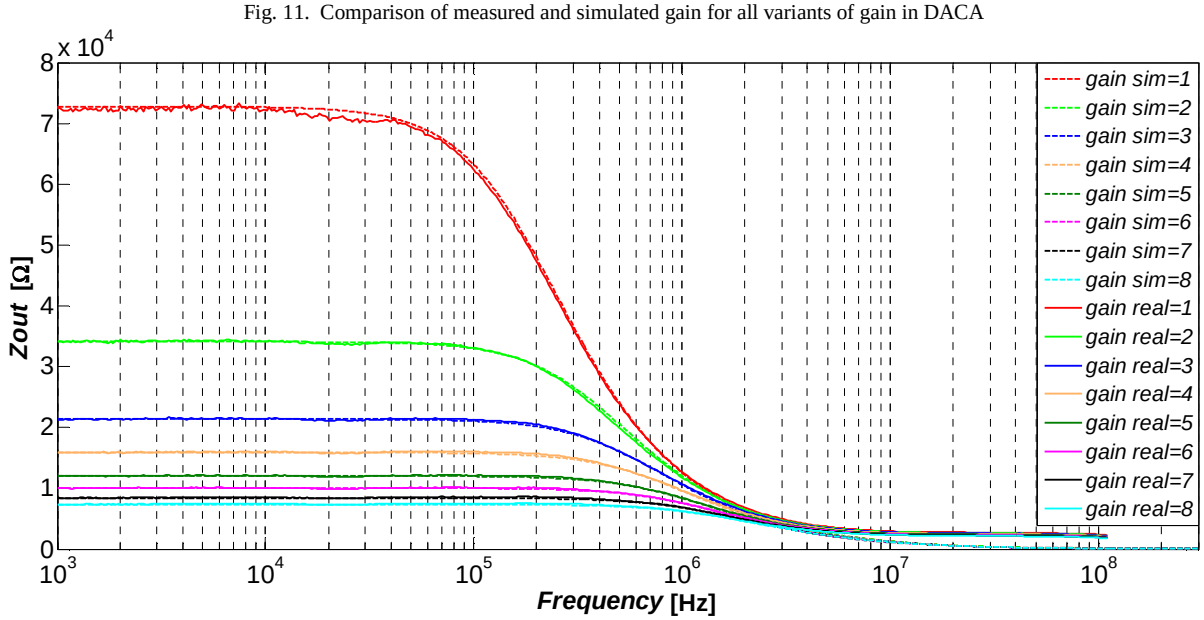

Fig. 12. Comparison of measured and simulated output impedance for all variants of gain in DACA

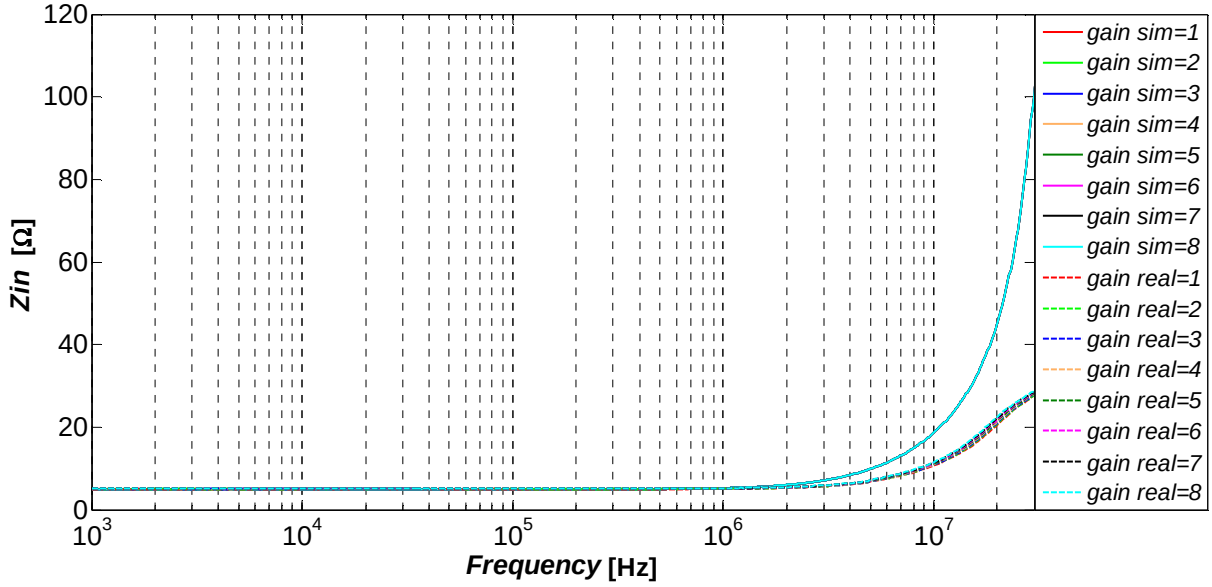

Fig. 13. Comparison of measured and simulated input impedance for all variants of gain in DACA

V. CONCLUSION

In this paper we presented an ABM model of recently developed digitally controlled current amplifier DACA. The ABM model of the active element is defined in four levels, each of which adds certain behavioural characteristics of the active element. The zero level is designed as a completely ideal and involves only an adjustment of gain from one to eight with a unity step. Gain selection is done by setting the value of the variable amplification (*gain*) from the specified range. The first level is based on the zero level, but the ideal gain values are replaced by real values and the level function reflects the influence of the input impedance (set to be constant; 5 Ω) and the output impedance (impedance value depends on the selected *gain*). The second level reflects the frequency dependence of the gain as well as frequency dependence of the input and output impedance. The third level of this model additionally reflects the input current limits (constant current limit value of 300 μA) and output current limit (particular limit value depends on the specified gain). These models are suitable to performance the initial simulations, where the operability of the proposed function blocks using DACAs as active elements is evaluated. Based on the simulation results, proper optimation steps can be done before experimental measurements are performed. Selected characteristics of the model and the real element DACA are presented in the form of graphs and are compared to each other.

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Network Protection Against DDoS Attacks

Petr Dzurenda, Zdenek Martinasek, Lukas Malina

***Abstract*—The paper deals with possibilities of the network protection against Distributed Denial of Service attacks (DDoS). The basic types of DDoS attacks and their impact on the protected network are presented here. Furthermore, we present basic detection and defense techniques thanks to which it is possible to increase resistance of the protected network or device against DDoS attacks. Moreover, we tested the ability of current commercial Intrusion Prevention Systems (IPS), especially Radware DefensePro 6.10.00 product against the most common types of DDoS attacks. We create five scenarios that are varied in type and strength of the DDoS attacks. The attacks intensity was much greater than the normal intensity of the current DDoS attacks.**

***Keywords*—Distributed Denial of Service Attacks, DDoS, Network protection, Security, Stress Testing, Cyberattacks.**

I. Introduction

Nowadays, cyberattacks have a significant role in the part of a computer crime. DDoS attacks are an integral part of these attacks. DDoS attack is a subset of a simpler and sometimes better known DoS (Denial of Service) attack. The main purpose of these attacks is to put targeted service to the nonfunctional state, it causes a denial of this service for regular users. A reason can be caused by bandwidth overload of the targeted server providing some services or any other resources. In some cases, an attacker can also get a targeted device to the inactive state. Attacks are usually aimed at web services or services of various organizations and corporations e.g. news servers, banks, government departments, enterprises etc. The main difference of DoS and DDoS attacks is in the line of attack. DoS attack uses only one network node (e.g. personal computer (PC) or server) and single Internet connectivity. The network node is directly under control of the attacker. On the other hand, the DDoS attack uses more than one network nodes and more than one Internet connectivity. These compromised network nodes are called zombies or botnets and they are not directly under the control of the attacker. It causes that the attack is consisted of large quantities of requests (usually hundreds or thousands), which can be realized from all over the world. The attacker usually creates a necessary infrastructure of botnets simply with using Trojan horses or other malware, which are running on infected network nodes of victims.

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Nowadays, any devices (e.g. personal computers, servers, smartphones etc.) which are connected to the Internet can become botnets. The basic principle of DDoS attack is depicted in Fig.1. The DDoS attack communication behaviour usually seems as a normal traffic. Hence, it is so hard to detect and to defense against this type of attack compared to simpler DoS attack. The DDoS attacks focus on a target nodes in a certain time and with a certain intensity of attacks. The intensity is much bigger than in DoS attacks. The recent DDoS incidents from 2009 to 2012 are listed in the work [1].

In 2013, two biggest DDoS attacks of history were made. The first attack was targeted at Spamhaus cyber-assault in March 2013. The attack had intensity of about 300 Gbps. In that time it was marked as ”the biggest cyberattack in the history”. In February 2014, the second attack with intensity about 100 Gbps higher than previously mentioned attack was realized. The attack had intensity of 400 Gbps and it was targeted at CloudFlare CEO Matthew Prince. However, most of DDoS attacks (more than 80%) have usually lower intensity about 50 Mbps with duration about half an hour.

Currently, the infrastructure of botnets is ready to begin an attack anytime. This is the reason why it is important to ensure maximum protection and security of every network infrastructure. The DDoS attack is able to cause not only damages due to denial of online services to users, but can also reduce the credibility of companies and their services.

In this paper, we test the ability of current commercial IPS system Radware DefencePro against current DDoS attacks. We tested its ability to detect and filter the most common types of the DDoS attacks, such as SYN flood, UDP fload, Reset flood and Xmas flood. Moreover, the realized attacks had intensity about 900 Mbps, which is much greater than current attacks usually have. The objective was to determine whether the device is able to withstand the current DDoS attacks.

II. Types of DDoS attacks

In this section, we describe and analyze the basic types of DDoS attacks. The types of DDoS attacks are dependent on the protocol where the attack is realized, for example HTTP (Hypertext Transfer Protocol), ICMP (Internet Control Message Protocol), UDP (User Datagram Protocol), TCP (Transmission Control Protocol), DNS (Domain Name System), SIP (Session Initiation Protocol). We distinguish attacks by impact on the targeted victim (bandwidth, memory, CPU) and cut-down services based on software bugs. According to the work [1], attacks can be distinguished to two basic types, flooding attacks and logical attacks.

A. Flooding attacks

This type of a DDoS attack is aimed at overloading the server resources such as bandwidth, memory or CPU by using

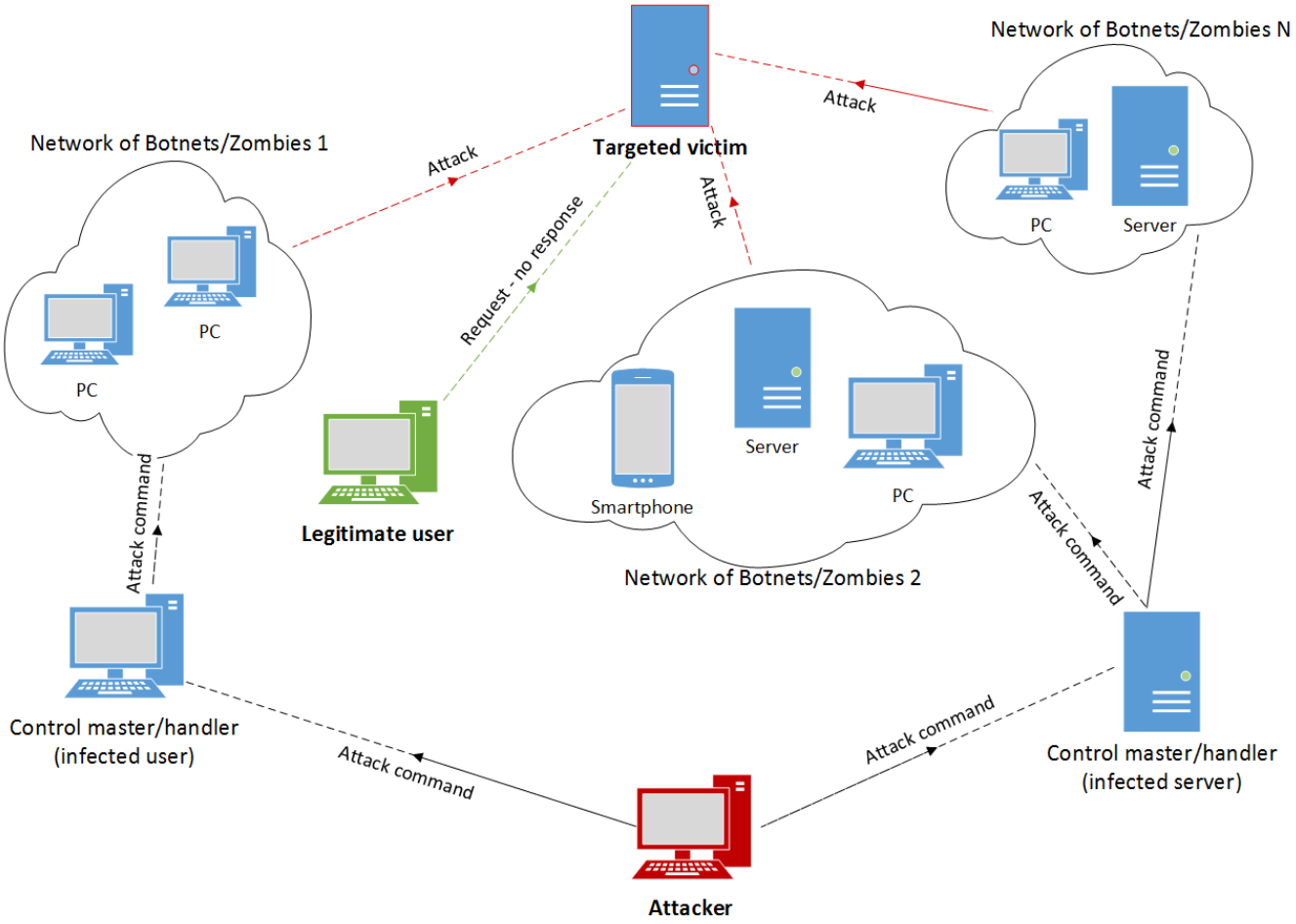

Fig. 1. The principle of a DDoS attack.

the large quantity of packets. This process causes a denial of service for the legitimate users. Flooding packets are usually implemented through the weaknesses of communication protocols (TCP, UDP, ICMP, FTP, SIP or HTTP). The most important flooding attacks are described below.

The SYN flood attack is the most common type of flooding attacks. It is based on half-open TCP connections. Classical TCP connection consists of 3-way handshake (SYN, SYN/ACK, ACK). During this attack, an attacker sends SYN packet with spoofed source IP address to the server (victim). The server reserves system resources for this potential connection and replies SYN/ACK to the spoofed IP address. The server waits for response ACK but it does not come. After some time, the server releases allocated resources. Strength of this attack depends on large quantities of SYN packets. The server exhausts its resources and it is not able to provide required services to legitimate users.

The UDP flood attack is based on sending large quantity of UDP datagrams that are targeted to random ports. A server (victim) tries to find some applications that listen on these ports. In case of no application listen, the server sends an ICMP message ”Destination unreachable”. The large quantities of UDP messages cause cut-down of the targeted system.

The ICMP flood attack is sometimes called *the Smurf attack* or *the Ping flood attack*. This attack sends a big amount of ICMP ECHO requests to the multicast IP address of any vulnerable network. A source IP address of the request is the same as the IP address of a victim. All nodes in this targeted network reply with an ICMP ECHO response message to the victim. The flood of ICMP ECHO responses cause an overload of the target system. The attack is realized on the network layer of TCP/IP. *The Fraggle attack* is similar to the ICMP flood attack, but it is realized on the transport layer of TCP/IP. The attack is based on using a UDP ECHO request (port 7) and a UDP Charge (port 19).

The ARP flood attack is based on flooding the targeted victim by spoofed ARP (Address Resolution Protocol) requests. It causes an exhaustion of computing and/or memory resources on the victim side. These types of attacks are suitable for use in a local network. Another way can be periodical sending of spoofed ARP responses (e.g. from network gateway) containing the IP address of the attacker. This attack is called *the ARP Spoofing Attack* and it realizes

known MITM (Man In The Middle) attack, when the all traffic is routed over the attacker.

The Xmas tree attack, an attacker generates so called Christmas tree packets, which have got set flags such as FIN, URG, and PSH in the TCP header. Processing these flags is difficult. This fact causes an overload of the targeted node in case of lots of incoming packets.

The Reset flood attack uses TCP packets, which contain a RST flag and spoofed source IP addresses. If lots of these packets are sent to victim's ports then there is a high probability that some existing connections will be reset.

The Unreachable host flood attack is similar to the Reset flood. An attacker sends an ICMP message "Host unreachable" to the random ports to the victim side and with a spoofed source IP address. There is a some probability that an existing session will be cancelled.

B. Logical attacks

Logical attacks aim at the weakness of applications or software on an targeted device. These attacks use small amounts of messages opposite to flooding attacks. The purpose is to get the targeted device to the non-functional state. The best known types are described below.

The Ping of death – an attacker sends a ping message with the data size higher than 65 535 b, which is maximum defined packet size in TCP/IP. The system running on targeted node tries to reassemble the packet. This may cause buffer overflow error and system may crash.

The Teardrop attack – an attacker sends two or more packet fragments with incorrect setting of offset. Fragments cannot be correctly reassembled to original packet. It often causes system crash.

The Land attack – an attacker sends a SYN packet to a victim. The packet has got spoofed source IP address and port, they are same as the victim's IP address and port. The victim tries to establish a connection to itself, which may cause its downfall.

Other types of attacks such as the DNS Query attack, the HTTP flood attack, the SIP flood attack etc. can be found in [1], [2] or in [3]. The recent versions of software systems eliminate many errors and weaknesses. However, it is necessary to periodically update these systems with actual security patches to protect them against existing logical attacks.

III. Detection of DDoS Attacks

Detection methods try to detect DDoS attacks in regular operations before a targeted device is affected. This early detection alerts the administrator of the targeted node, which can reduce the consequences of the attack to a minimum. It can be ensured by using a network security device or/and by using well-designed load balancing. Generally, the detection methods are divided as signature and anomaly detection.

A. Signature detection

The detection methods using the signatures are based on the good knowledge of DDoS attacks. Usually, the characteristics are manually constructed by a group of experts, and signatures are implemented to security and surveillance network devices. Monitoring the packet headers by firewalls, routers or Intrusion Detection Systems (IDS) helps to recognize the symptoms of incoming DDoS attacks. Signature detection methods are effective only against known types of DDoS attacks. Therefore, these detection mechanisms do not recognize new and unknown attacks. The most commonly used detection methods or symptoms are presented in [4], [5].

B. Anomaly detection

Some types of DDoS attacks are detected and classified by finding anomalies in the network traffic. For example, flood attacks using TCP-SYN, UDP or ICMP packets increase of these packets can be observed. These detection methods are trying to find some anomaly in the normal network traffic. The work [6] shows the possibility of using artificial intelligence such as neural networks and genetic algorithms to detect unusual network traffic and the classification of DDoS attacks in the normal network traffic. At first, this artificial intelligence learns how normal network traffic seems and then it tries to detect differences between them. Authors of work [7] use detection technique based on a decomposition of time series. Work [8] uses covariance analysis model for SYN flooding attacks detection and in works [9], [10], entropy-based method are used. The disadvantage of these detection methods is often a larger number of false alarms. On the other hand, these methods are able to recognize new types of attacks.

IV. Protection against DDoS attacks

Generally, a DDoS defense mechanism consists of four basic parts. At first, it is a DDoS prevention. The attack detection is the next part. This part determines the source of the attack and classifies malicious packets in the network traffic. The next part is a reaction that is designed to stop an attack, or to limit the damage caused by the effects of the attack. This involves dropping the malicious packets or providing the services on the backup device/line or ensuring the partially availability of the services by using the Quality of Service (QoS). All these actions must not influence regular traffic. The proposal of a complex security solution that is suitable for a defense against all known and unknown DDoS attacks is very difficult. DDoS defense solutions can be maintained by the sophisticated combination of a robust network infrastructure, including an active security network equipment such as firewalls, honeypots, IDS sensors (Intrusion Detection System) or IPS (Intrusion prevention System) which are capable of DDoS attack detection and providing the defense of a protected network/server. The flexible management

and supervision are often also important. It is also important to establish emergency scenarios in case of a DDoS attack. The basic methods and techniques which can partially eliminate DDoS threats are described in the following sections.

A. Network infrastructure security

A secure network infrastructure should consist of network security devices such as routers, firewalls, IDS systems or better IPS systems and so called honeypots. The main purpose of honeypots is to create a fake weakness in the infrastructure. This honeypots could be potentially attacked and it detects these attacks. Some DDoS attacks can be detected in real time using detection components as IDS systems. The malicious packets are filtered by the firewall. Border routers can also reduce the impact of DDoS attacks on the protected network or server. Redundant lines and servers can mitigate DDoS attacks and ensure access for authorized users. These basic defense types are presented in [11], [12] or in [13].

B. Black and white lists protection

Simple security solutions against DDoS attacks are presented in [14]. Transactions and request packets from legitimate users are shifted to the backup link. The IP addresses of authorized users are stored on the "whitelist" after successful authentication. If the IP addresses are detected as suspicious, they are stored on "blacklist". This type of defense may contain two firewalls, which are controlled by one management system that manages both sheets.

C. Defense by using offensive methods

In [15], the authors present a method which reduces the effect of DDoS attacks by using the offensive approach. The principle of this approach is based on increasing the number of request packets from legitimate users. Due to this fact, the legitimate user receives the response from the server with higher probability. This defensive technique is only effective for a small group of DDoS attack types.

V. Realized experiments

This section contains the description of security tests and the results from Radware DefensePro 6.10.00 against the most common DDoS attacks, such as SYN flood, UDP flood, Reset flood and Xmas flood. The test results serve as a feedback that shows the need to protect a network against these types of attacks. Furthermore, the configuration of the DDoS filter and its efficiency for network protection are presented here.

A. Security testing

In this security test, IPS (Intrusion Prevention System) Radware DefensePro is tested by using the network tester/generator (stress tester) Spirent Avalanche 3100B against the influence of the DDoS attacks. The tester enables the comprehensive testing of a network infrastructure based on IP protocol. The tester is able to generate real traffic up to 20 Gbps (2x10 GbE) and allows the emulation of network clients and servers on layers L4 – L7. The stress tester offers 15 types of DDoS attacks. A software component Attack Designer allows us to build own attacks. As a tested device, which provides a protection against DDoS attacks, Radware DefensePro 6.10.00 has been used. This device is able to detect and filter DDoS attacks up to 12 Gbps in real time. The filter supports technologies 10 Gb and 100 Gb Ethernet. The device has one management port, which is used for getting reports. To get the reports some management interfaces for example APSolute Vision, web interface and a console interface can be used. DefensePro provides the following security protection:

Network-wide protection – includes the following:

1) *Behavioral DoS* – protection against zero-day flood attacks, including SYN floods, TCP floods, UDP floods, ICMP and IGMP floods.
2) *Scanning and worm protection* – zero-day protection against self-propagating worms, horizontal and vertical TCP and UDP scanning, and ping sweeps.
3) *SYN protection* – protection against any type of a SYN flood attack using advanced SYN cookies. The SYN flood attack is usually aimed at specific servers with the intention of consuming the server's resources. However, the configuration of the SYN protection as a network protection allows easier protection of multiple network elements.

Server protection – includes the following:

1) *Connection limit* – protection against session-based attacks, such as half open SYN attacks, request attacks and connection attacks.
2) *Server-cracking protection* – zero-day protection against application-vulnerability scanning, brute-force and dictionary attacks.
3) *HTTP Mitigator* – mitigates zero-day HTTP page flood attacks.

Signature-based protection – protection against known application vulnerabilities and common malware, such as worms, trojans, spyware, and DoS.

Access Control List – provides stateful access control.

The block scheme of the security testing testbed is depicted in Fig. 2. The scheme consists of the stress tester (Avalanche 3100B), the tested device (Radware DefensePro 6.10.00), a management server APSolute Visio and a control terminal. The control terminal is used to configure both the tester and the filter, and to display results and characteristics obtained during the test. Two 10 GbE ports of the tester (Port12 and Port13) have been used during testing. The first port has been configured to generate the legitimate traffic and, in addition, some types of DDoS attacks. The second port has been configured to emulate the servers of selected protocols. Five scenarios for FTP (File Transfer Protocol) and HTTP (Hypertext Transfer Protocol) application-layer protocols have been created. The Radware filter has been connected between the ports and configured to filter the DDoS attacks while leaving the legitimate traffic without any modification. For each scenario, the test has been run with the deactivated filter. Then, the filter has been activated. The goal of testing has

been to evaluate how helpful the filter Radware is in a DDoS attack mitigation.

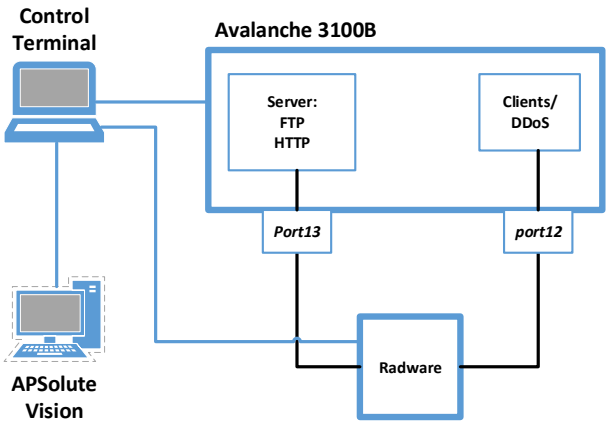

Fig. 2. Block scheme of the security testing testbed.

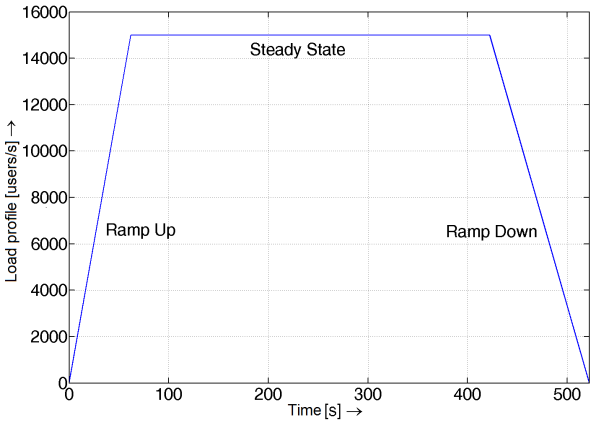

Fig. 3. FTP and HTTP load profile graphs.

B. Scenario specification

In each created scenario (a security test), the stress tester is used for simulating both communicating parties, users and servers. The Port12 is configured to generate the client traffic and the DDoS attack on the IPv4 network. The Port13 is used to emulate the servers with respective services on standard ports on the IPv4 network. In each tested scenarios, a single 1 kB file is repeatedly transferred using the FTP protocol from a server listening on ports 20, 21 and at the same time a web-page is repeatedly transferred using the HTTP protocol from a server listening on the port 80. On this regular network traffic, we apply different types of DDoS attacks such as DDoS SYN flood, UDP flood, Reset flood a Xmas flood. In first four scenarios, attacks are applied separately and in the fifth scenario they are applied together.

In all scenarios, the load profile is specified by the number of users performing defined actions per second during the entire test. In testing scenarios, each user performs FTP file transfer of size 1 kB and loads a web page. This load is specified in the tester by a load profile. The load profile graph contains the Ramp Up, Steady State and Ramp Down sections as depicted in Fig. 3 for the FTP and HTTP scenario. The detailed information regarding specification of the individual scenarios are presented in the Tab. I.

C. Achieved results

The results of the security tests of the Radware DefensePro 6.10.00 are obtained by using the Avalanche Commander, Spirent Avalanche Analyzer and APSolute Vision. The graphical representation of all scenarios results with the filter disabled is depicted in Fig. 4. In the graphs, the success rate of the application-layer transactions is depicted for all tested scenarios depending on the type and intensity of DDoS attack. The protocols success rate is 38% in the case of DDoS SYN flood attack, successful transfer for UDP flood is 80%, in case of Reset flood it is 78% and for Xmas flood it is 88%, when the DDoS attack is deployed. The fifth graph describes the successful transfer in case of an attack, when all attacks are applied together to the regular network traffic. The success rate is only 12%. The graphical representation of all scenarios results with the filter enabled is depicted in Fig. 5. All the scenarios have success rate of 100% if the filter is enabled. The results show the positive impact of the DefensePro 6.10.00 filter. The DDoS attack is completely mitigated and the network infrastructure is fully functional if the filter is enabled. All results were obtained from the Spirent Avalanche device.

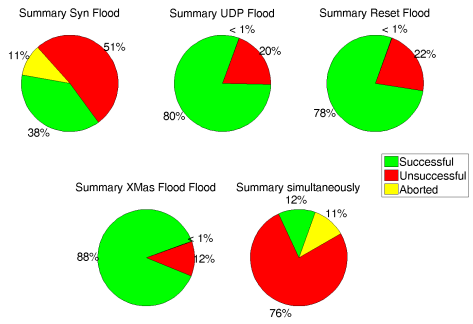

Fig. 4. Summary results for the disabled Radware DefensePro filter.

Tab. II and Tab. III show the numerical values of all tests, with the disabled and enabled filter. The tables contain the number of total successful, unsuccessful and cancelled transactions.

The results obtained from Radware DefensePro with using APSolute Vision are depicted in Fig. 6. DefensePro detects all four DDoS attacks aimed at the protected network in fifth tested scenario. The security threat of an attack is marked as ”HEAVY” and the category of an attack is detected as ”Packets Anomalies”. This means that DefensePro detects some anomalies in the network traffic (in this case increasing of network traffic) see section III-B. Network traffic (regular

TABLE I
TEST SPECIFICATION.

Client	
Physical port	Port12
Line speed	10 Gbps
Packet loss	0%
FTP, HTTP load	15 000 users/s
Protocols	FTP/HTTP
Network address/mask	192.168.0.0/16
Address space	192.168.1.17–192.168.255.254
Server	
Physical port	Port13
Line speed	10 Gbps
Packet loss	0%
FTP	
Server port	FTP(21)
Network address/mask	192.168.1.0/28
Server address	192.168.1.1
File size	1 kB
HTTP	
Server type	Apache/2.0.49
Server port	HTTP(80)
Maximum requests	64
Network address/mask	192.168.1.0/28
Server address	192.168.1.6
File	index.html
File size	566 kB
DDoS attack 1. – 4. scenarios	
Type	SYN flood, UDP flood,
	Reset flood, Xmas tree
Packets sent	18 000 000
Attack duration	180 s
DDoS attack 5. scenario	
Type	SYN flood
Packets sent	22 000 000
Attack duration	220 s
Type	UDP flood
Packets sent	18 000 000
Attack duration	180 s
Type	Reset flood
Packets sent	10 000 000
Attack duration	100 s
Type	Xmas tree
Packets sent	12 000 000
Attack duration	120 s

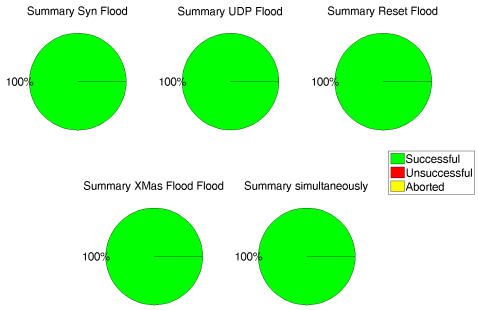

Fig. 5. Summary results for the enabled Radware DefensePro filter.

traffic and traffic represented by DDoS Attacks) traversing through Radware is shown in Fig. 7. Legitimate traffic is marked in green. This traffic is released to output without any modifications and it corresponds to the load profile of the Avalanche tester see Fig. 3. On the other hand, individual attacks, which have been started in the different time have been detected and filtered. This illegitimate traffic is marked in red. The graph marked in blue describes the increase of network traffic on the input port, which is caused by applying DDoS attacks.

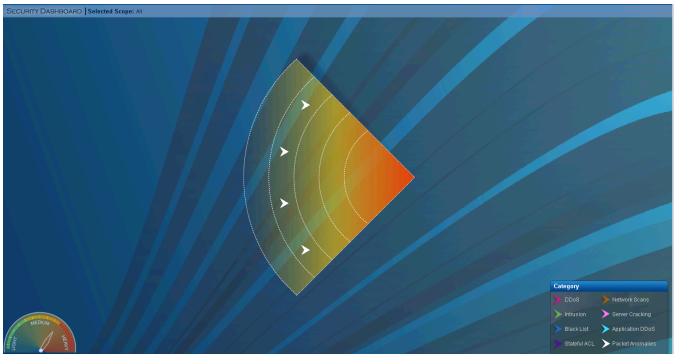

Fig. 6. DDoS attacks detection by Radware DefensePro.

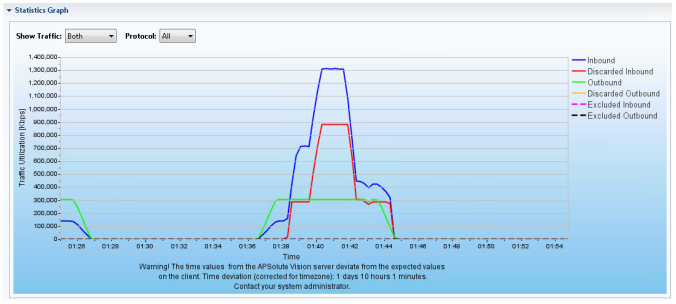

Fig. 7. Detection and filtering of DDoS attacks by Radware DefensePro in real time.

VI. CONCLUSION

In this paper, we presented basic information about DDoS attacks, their types and methods of DDoS detection and defense. In these days, there are several security solutions against DDoS attacks. A well-established security solution is usually a combination of prevention, good infrastructure with network security devices, backup resources and sophisticated crisis scenarios in the case of a DDoS attack.

In the paper, we described our testing implications of DDoS attacks on the quality of the service, such as FTP and web services. Furthermore, we tested a DefensePro 6.10.00 device from Radware company which is able to detect and filter many types of network attacks, including DDoS attacks in real time. We created five scenarios, which were aimed at the different types of DDoS attacks with a different intensity. In the first four scenarios, we implemented attacks as SYN flood, UDP flood, Reset flood and Xmas flood separately. In case of the fifth scenario, we applied all attacks from the previous scenarios together. In all scenarios, we tested the influence of

TABLE II
SUMMARY RESULTS FOR THE DISABLED DEFENSEPRO FILTER.

	Syn Flood	Udp Flood	Reset Flood	Xmas Flood	All
Total transactions	10663760	10592631	10408262	11331240	11137990
Successful transactions	4041351	8499729	8126965	10006739	1383676
Unsuccessful transactions	5489351	2087108	2274594	1320481	8508772
Canceled transactions	1133058	5794	6703	4020	1245542

TABLE III
SUMMARY RESULTS FOR THE ENABLED DEFENSEPRO FILTER.

	Syn Flood	Udp Flood	Reset Flood	Xmas Flood	All
Total transactions	10663760	10592631	10408262	11331240	11137990
Successful transactions	10663760	10592631	10408262	11331240	11137990
Unsuccessful transactions	0	0	0	0	0
Canceled transactions	0	0	0	0	0

a protected network with disabled or enabled DDoS protection services. The results of security tests show that DefensePro is able to filter all the DDoS attacks of difference types and intensity. Furthermore, the device is able to withstand the DDoS attack on the minimum intensity of about 900 Mbps, it is 18 times more than the current attacks usually have.

ACKNOWLEDGMENT

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History, Progress and New Results in Synthetic Passive Element Design Employing CFTAs

Jaroslav Koton, Norbert Herencsar, and Martin Venclovsky

***Abstract*—After the presentation of the Current Follower Transconductance Amplifier (CFTA) active element, it has found a numerous application possibilities while designing linear and non-linear analog function blocks. This paper gives a short review of the CFTA and mainly focuses on the synthetic floating and grounded passive element design, which can also be electronically controllable. Except the design of synthetic inductors, also possible realizations of floating and grounded capacitors and resistors are described, where the value of these passive elements can be adjusted by means of active elements' parameters. For the design of the corresponding circuit realizations, the Mason-Coates signal flow graph approach is used. The performance of some discussed synthetic elements is verified and evaluated by Spice simulations on simple analog frequency filters.**

***Keywords*—CFTA, synthetic inductor, synthetic capacitor, synthetic resistor, frequency filter, signal processing.**

I. Introduction

Even if in these days the signal processing is mainly performed in the digital form, analog function blocks are still required in front-end interfaces. Probably the most discussed and used function blocks are the analog passive or active frequency filters, where in the literature more attention is paid to active ones. Although the mathematical description of these function blocks is very well known and the number of described circuit solutions using different types of active elements is also quite high, the engineers are still looking for new challenges if low supply voltage, low power consumption, or low noise are to be considered. Hence, new or modified active elements and new frequency filter design approaches are presented in the literature.

Once assuming the variety of active elements, probably the best known are the operational amplifiers (OPAs) and operational transconductance amplifiers (OTAs). These active elements are considered to be used in voltage mode (VM) function blocks, i.e. both the input and output variable to be voltage. However, other active elements suitable for the design of analog function blocks are discussed in the literature, such as Current Conveyors (CC) and their first generation - CCI [1], second generation - CCII [2] and third generation - CCIII [3], Voltage Conveyors (VC) [4] and their variants such as Current Differencing Buffered Amplifier (CDBA) [5] or Universal Voltage Conveyor (UVC) [6]. Even if these active elements have both voltage and current input and/or output terminals, they are mostly used in function blocks working in the current mode (CM), where the input and output signal is represented by current. However, the character of the input and output variable of a function block does not have to be necessarily the same and hence mixed mode function blocks are designed that are described by a transadmittance or transimpedance transfer function. Interconnecting conveyors and/or voltage followers (VF) and/or current followers (CF) and operational transconductance amplifiers other types of active elements are presented in the literature with the aim of simpler internal transistor implementation. The Current-Differencing Transconductance Amplifier (CDTA) [7], Current Conveyor Transconductance Amplifier (CCTA) [8], Current Through Transconductance Amplifier (CTTA) [9] or Current Follower Transconductance Amplifier (CFTA) [10] can be given.

While presenting new types of active elements, their application possibilities are mostly shown on the design of frequency filters. For the design of linear functional blocks with these active elements, a number of methods can be used. The autonomous circuit method [11], [12], adjoint transformation [13], the use of passive prototype [14], or signal flow-graph approach [15] can be mentioned as examples.

This paper deals with the idea of designing synthetic elements that with advantage can be employed in passive filtering structures. For this purpose, the CFTA is used as active element for sake of the synthetic elements design. The paper is organized as follows: first, in section II the CFTA active element is described and possible realizations for practical verifications are given; next, in section III using signal flow graph approach, the circuit solutions of floating and grounded passive elements are discussed; in section IV, some of the synthetic elements are employed in simple function blocks to show their performance; section V concludes this paper and gives some views of future work in area of CFTA usage in analog signal processing blocks.

II. CFTA - Current Follower Transconductance Amplifier

A. Active Element Description

The Current Follower Transconductance Amplifier (CFTA) (Fig. 1(a)) is an analog active element that has been presented in [10] as a simplified version of the CDTA [7]. The simplification of CDTA to CFTA consists in the reduction of one low-impedance current input (n) as it can be seen from Fig. 1. The reason of such simplification was the fact that in

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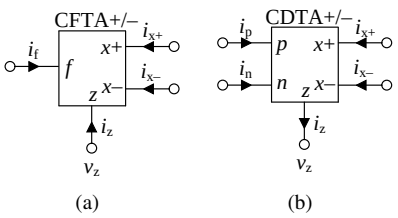

Fig. 1. Circuit symbols of (a) CFTA, (b) CDTA

numerous circuit solutions using CDTAs p or n terminals of individual active elements remain unconnected [7], [16]-[23] and hence can cause undesired noise injection into the circuit and subsequently increase the noise level at the output of the function block. Therefore, the CFTA uses only single low-impedance current input denoted as f, two high-impedance current outputs $x+$ and $x-$ and one auxiliary high-impedance voltage terminal z. The relation between the terminal currents and voltages of this active element can be described by following hybrid matrix:

$$\begin{bmatrix} v_f \\ i_z \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ \alpha & 0 & 0 & 0 \\ 0 & g_m & 0 & 0 \\ 0 & -g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} i_f \\ v_z \\ v_{x+} \\ v_{x-} \end{bmatrix}, \qquad (1)$$

where $\alpha = 1-\varepsilon$ is the current gain from the f terminal to the z terminal and g_m is the transconductance of the active element, whereas $|\varepsilon| << 1$ is the current tracking error. Generally, the g_m and α are frequency dependent, however for sake of simplicity, in following sections ideal values are assumed, i.e. g_m being constant and α being unity.

From the behavioral point of view, the CFTA can be represented as an interconnection of the Current Follower (CF) and Balanced-Output Transconductance Amplifier (BOTA) as it is shown in Fig. 2. The input of the current follower corresponds to the input terminal f of CFTA Fig. 2(a). The output of the current follower is interconnected with the negative voltage input of BOTA whereas this node also represents the auxiliary voltage input z. Based on the transconductance g_m of BOTA, the voltage at the z terminal is converted to corresponding currents i_{x+} and i_{x-}. Thanks to the usage of BOTA, there is a potential of the transconductance g_m being electronically tuned [24]. Therefore, the parameters of function blocks employing CFTA elements might be also tuned once proper CMOS implementation of the CFTA is used [25]. Based on the description of the behavior of the CFTA, its basic CMOS implementation can be used as shown in Fig. 2(b) [26]. Other possible CMOS or bipolar implementations of CFTA can be found e.g. in [27], [28].

In Fig. 3(a) possible implementation of CFTA using readily available integrated circuits is shown. Here, to implement the current follower, the current feedback amplifier AD844 [29] is used. The current follower can be also implemented using e.g. OPA861 [30]. The second part of CFTA represented by an OTA can be implemented using MAX435 [31]. Possible realization of a multiple-output CFTA (MO-CFTA) is shown in Fig. 3(b) [32], where the second generation current

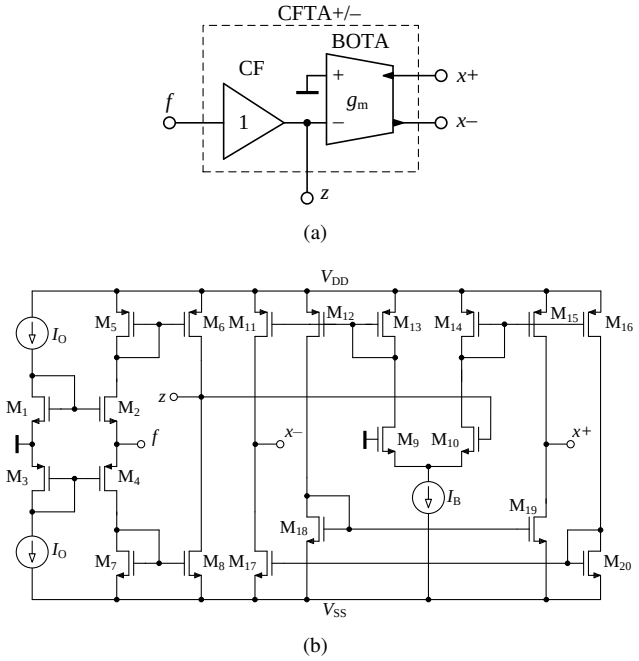

Fig. 2. Implementation of CFTA (a) interconnecting CF and BOTA, (b) CMOS implementation [26]

conveyor CCII+/– and Universal Current Conveyor (UCC) are used. Such interconnection is suitable for experimental measurements as the UCC together with CCII are part of the UCC-N1B integrated circuit, which in cooperation with Brno University of Technology has been designed by ON Semiconductor Ltd. [33], however, it is currently available only in laboratory samples. Note that in Fig. 3(b) using the Z_{S-} instead of Z_{S+} as an output terminal z, the MO-ICFTA (Multiple-Output Inverting CFTA) [34], which is also referred to as MO-CITA (Multiple-Output Current Inverter Transconductance Amplifier) [35], can be simply implemented using UCC-N1B.

B. Active Element Application Possibilities

Since the presentation of the CFTA, it has found its application possibilities in both linear and non-linear analog signal processing and function block design.

Mainly, it is employed in current- and voltage-mode multifunction frequency filters [10], [25], [27], [28], [32], [36]-[55]. E.g. in [32] three CFTAs are used to realize a current-mode single-input-multi-output second-order filter that features pole-frequency adjustment without varying quality factor of the pass-band gain. In the literature, research results that focus just on all-pass frequency filter design can be also found [56]-[60].

The proposed all-pass filters can be subsequently used for the design of oscillators as it is shown in [57] and [58]. However, the CFTA can be also used for direct quadrature and multi-phase oscillator design as presented in [61]-[67].

Assuming non-linear function blocks, the CFTA has been used to implement square-rooting circuits, multipliers, dividers, half-wave and full-wave rectifiers [68]-[72].

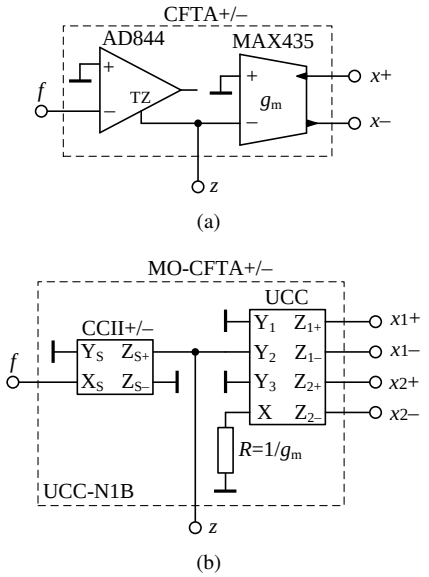

Fig. 3. Implementation of CFTA using (a) AD844 and MAX435, (b) Universal Current Conveyor (UCC)

Following the purpose of this paper, the current follower transconductance amplifier has found its application possibilities also in synthetic element design. The main focus is on the design of floating or grounded lossy or lossless inductor simulators [73]-[78]. In [73] using three CFTAs, the floating lossless inductor simulator is presented that can be easily used to design a grounded lossless inductor. Furthermore, in [73] using four active elements a floating capacitor simulator is presented. Simplifying the circuit solution of the floating inductor simulator from [73], the grounded lossless inductor using only two active elements and single grounded capacitor is presented in [74]. Using the V-I signal flow graph approach, the structure of grounded inductor simulator is presented in [75], which is, however, the same as in [74]. To reduce the number of active elements in floating lossless inductance simulator in [73], a modified version of CFTA, namely the Z-copy CFTA has been used. The structure in [76] uses only two active elements and single grounded capacitor, however, an external resistor is required. The grounded lossless inductor simulator of minimal configuration is presented in [77]. The solution is generally based on the circuit presented in [76], where the external resistor is now assumed to the intrinsic resistance of the active element - the CCCFTA (Current Controlled Current Follower Transconductance Amplifier). So far, the most complex paper dealing with the basic synthetic element design using CFTAs is [78], where the circuit solutions of inductor simulator, capacitance multiplier and also resistor simulator both floating and grounded are presented. However, in some cases the solutions presented in [78] operate only with ideal active elements. Following our previous results presented in [79], using the M-C signal flow graph approach, in this paper we present the design procedure of synthetic elements, where alternative and correct circuit solutions of basic synthetic elements are discussed.

III. Floating and Grounded Synthetic Elements Design

While designing synthetic elements, the researchers mainly focus on the design of lossless or lossy grounded or floating synthetic inductor. The theory of synthetic elements can be further generalized where also other basic passive element interconnections can be realized using active elements to provide e.g. simple electronic adjustment of the designed function block's parameters.

Here, once designing floating and grounded synthetic passive element, not only the the final circuit solutions are presented but also using the M-C signal flow representation of the passive components corresponding active circuit solution is determined.

A. M-C signal flow Graph Theory

Generally, a M-C signal flow graph is more used for sake of analysis of some known circuit rather than for a synthesis. However, e.g. in [15], the advantage of the signal flow graph design approach has been shown. To determine a relation or transfer function between two selected nodes (input X and output Y) in a graph the Mason's gain formula [80]:

$$K = \frac{Y}{X} = \frac{1}{\Delta}\sum_i P_i \Delta_i \tag{2}$$

should be used, where P_i is the transfer of the ith direct path from the input node X to the output node Y, and Δ is the determinant of the signal flow graph:

$$\Delta = V - \sum_k S_1^{(k)} V_1^{(k)} + \sum_l S_2^{(l)} V_2^{(l)} - \sum_l S_3^{(m)} V_3^{(m)} ..., \tag{3}$$

where V is the product of the self-loops, $S_1^{(k)}$ is the transfer of the kth oriented loop and $V_1^{(k)}$ is the product of all self-loops not touching the kth oriented loop; $S_2^{(l)}$ is the transfer product of two mutually not touching oriented loops and $V_2^{(l)}$ is the product of the self-loops not touching the lth oriented loops. In case that an oriented loop or kth direct path is touching all nodes, then the product V or Δ_k is unity. In (2) Δ_i is the determinant of that part of the graph that is not touching the ith direct path.

It can be obvious that except the knowledge of the Mason's gain formula, it is also necessary to know the corresponding M-C graph of the active element. According to (1) the reduced M-C flow graph of the CFTA active element is shown in Fig. 4, where ideal behavior of the active element is assumed, i.e. $\alpha = 1$. In Fig. 4 Y_i represents the sum of admittances connected to the corresponding (i) terminal of the active element.

Based on the signal flow graph of the basic passive elements, and in some cases of their parallel interconnection, using the CFTA corresponding M-C flow graphs representing an active solution of the immittance simulator are determined.

B. Floating Lossless Inductor Simulator

To define the equivalent active solution of a floating inductor, the general admittances Y_A and Y_B are used as shown in Fig. 5. These general admittances represent parts of the circuit

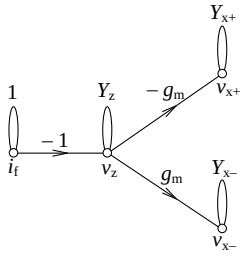

Fig. 4. Reduced M-C signal flow graph of CFTA+/-

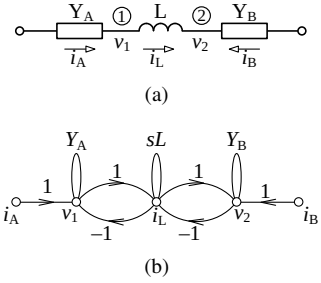

Fig. 5. (a) Floating passive inductor connected in to a circuit (represented by admittances Y_A and Y_B), (b) corresponding signal flow graph

that are interconnected with the inductor. In the corresponding signal flow graph (Fig. 5(b)), the general admittances at the input and output of the inductor are present only to show their influence on the gain of the corresponding self-loops. Using (2) following transfer function can be obtained:

$$\frac{v_1}{i_B} = \frac{v_2}{i_A} = \frac{1}{sLY_AY_B + Y_A + Y_B}, \tag{4}$$

which generally corresponds to a floating element.

Before presenting the determined signal flow graph of the active inductor simulator, it is suitable to shortly describe the features of the signal flow graph from Fig. 5(b). Once assuming the input and output node according to (4) there is only single direct path between these nodes and the signal flow graph consists only of two mutually touching oriented loops. Such properties should also feature the signal flow graph of the inductance simulator using CFTAs.

In Fig. 6(a) the signal flow graph of the active lossless floating inductor simulator is shown. This signal flow graph also generally consists of two mutually touching oriented loops and the using (2) the transfer function can be found as:

$$\frac{v_{z3}}{i_A} = \frac{g_{m1}g_{m2}}{sC_LY_AY_B + Y_Ag_{m2}g_{m3} + Y_Bg_{m1}g_{m2}}, \tag{5a}$$

$$\frac{v_{z1}}{i_B} = \frac{g_{m2}g_{m3}}{sC_LY_AY_B + Y_Ag_{m2}g_{m3} + Y_Bg_{m1}g_{m2}}, \tag{5b}$$

which in general corresponds to (4) and once we assume:

$$C_L = Lg_{m1}g_{m2}, \tag{6}$$

while $g_{m1} = g_{m3}$ then (4) and (5) become identical. According to Fig. 6(a) the circuit representation of the floating inductor simulator using three CFTAs (being identical with the solution

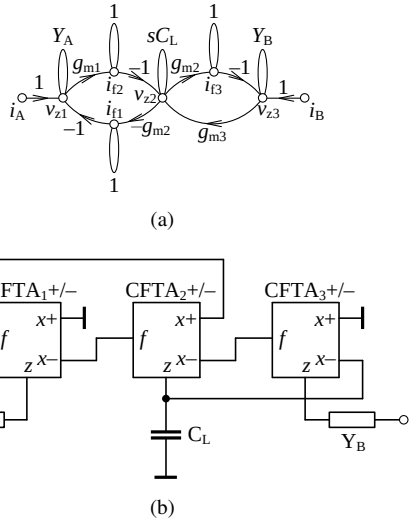

Fig. 6. (a) Signal flow graph of the floating inductor simulator using CFTAs, (b) circuit representation

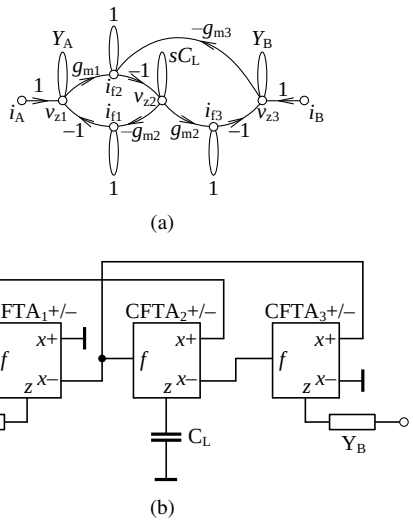

Fig. 7. Optimized solution of the floating inductor simulator using CFTAs: (a) signal flow graph, (b) circuit representation

presented in [78]) is shown in Fig. 6(b), whereas the equivalent inductance is determined as:

$$L_{eq} = \frac{C_L}{g_{m1}g_{m2}}, \tag{7}$$

once $g_{m1} = g_{m3}$.

The structure of the floating inductor simulator in Fig. 6 can be further optimized as it is shown in Fig. 7. In practice this optimization results in better performance of the inductor simulator at higher frequencies as the capacitor C_L is connected only to the z terminal of CFTA$_2$.

C. Grounded Lossless Inductor Simulator

The circuit solution of an grounded lossless inductor simulator can be determined from Fig. 6 or Fig. 7. Using the signal flow graph approach, the assumed representation of a passive inductor connected to a circuit together with the corresponding signal flow graph is shown in Fig. 8.

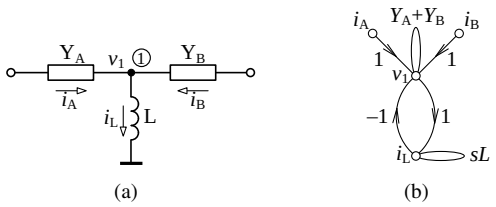

Fig. 8. (a) Grounded passive inductor connected in to a circuit, (b) corresponding signal flow graph

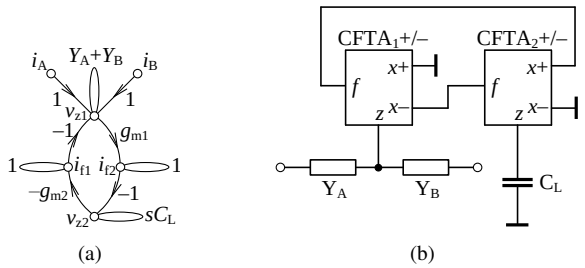

Fig. 9. (a) Signal flow graph of the grounded inductor simulator using CFTAs, (b) circuit representation

The transfer function of the signal flow graph is:

$$\frac{v_1}{i_B} = \frac{sL}{sL(Y_A + Y_B) + 1}. \tag{8}$$

Following the features of the signal flow graph from Fig. 8(b), signal flow graph using active elements can be defined as shown in Fig. 9(a). The transfer function of signal flow graph of the grounded inductor simulator can be determined as:

$$\frac{v_{z1}}{i_B} = \frac{sC_L}{sC_L(Y_A + Y_B) + g_{m1}g_{m2}}. \tag{9}$$

Assuming (6), then (9) and (8) become identical and hence the circuit solution in Fig. 9(b) represents an active simulator of a grounded lossless inductor with the equivalent inductance given by (7).

D. Floating Capacitor Multiplier

Generally, it is not difficult to produce neither grounded or floating capacitor in the integrated form nowadays. However, based on the technology used the capacitance of such capacitors is limited to tents of pF. Therefore, capacitor multiplies are useful function blocks once higher capacitances have to be used. Furthermore, using suitable active elements, the value of the capacitor can be easily adjusted, if required.

To derive the active floating capacitor multiplier, a floating capacitor C is assumed as shown in Fig. 10. The transfer function of the signal flow graph from Fig. 10(b) can be determined as:

$$\frac{v_1}{i_B} = \frac{v_2}{i_A} = \frac{sC}{sCY_A + sCY_B + Y_AY_B}. \tag{10}$$

As it is obvious from Fig. 10(b) the signal flow graph has only single oriented loop with the gain s^2C^2, which is typical for floating passive elements represented as admittances in a graph. Therefore, to avoid the use of a floating capacitor in the active capacitor multiplier and still obtain the transfer function sufficient number of terms, the signal flow graph must contain of three mutually touching loops and furthermore, the corresponding signal flow graph must contain a high-impedance node, which in Fig. 11(a) is characterized by zero self-loop gain.

The transfer characteristic of the signal flow graph from Fig. 11(a) is:

$$\frac{v_{z3}}{i_A} = \frac{sC_g g_{m1} g_{m_2}}{sC_g g_{m2}(Y_A g_{m3} + Y_B g_{m1}) + Y_A Y_B g_{m4} g_{m5}}, \tag{11a}$$

$$\frac{v_{z1}}{i_B} = \frac{sC_g g_{m2} g_{m_3}}{sC_g g_{m2}(Y_A g_{m3} + Y_B g_{m1}) + Y_A Y_B g_{m4} g_{m5}}. \tag{11b}$$

Comparing (10) and (11) the equivalent value of the floating capacitor can be determined as:

$$C_{eq} = \frac{g_{m1}g_{m2}}{g_{m4}g_{m5}} C_g, \tag{12}$$

while it must hold $g_{m1} = g_{m3}$.

Comparing the circuit solution of the capacitor multiplier from Fig. 11(b) (or its signal flow graph in Fig. 11(a)) to the floating inductor simulator from Fig. 6(b) and the grounded inductor simulator from Fig. 9(b) it can be observed that the capacitor multiplier represents an interconnection of the floating inductor simulator, where instead of a capacitor C_L the grounded inductor simulator is connected. This feature fully corresponds to the circuit theory, e.g. [81].

Similarly, as the floating inductor simulator has been optimized, also an optimized solution of the capacitor multiplier can be described as shown in Fig. 12(b). Furthermore, using MO-CFTA, the number of active elements could be limited by one. This optimization step can be more obvious from the signal flow graph in Fig. 12(a) that has the transfer function defined as:

$$\frac{v_{z3}}{i_A} = \frac{sC_g g_{m1} g_{m_2}}{sC_g g_{m2}(Y_A g_{m3} + Y_B g_{m1}) + Y_A Y_B g_{m2} g_{m4}}, \tag{13a}$$

$$\frac{v_{z1}}{i_B} = \frac{sC_g g_{m2} g_{m_3}}{sC_g g_{m2}(Y_A g_{m3} + Y_B g_{m1}) + Y_A Y_B g_{m2} g_{m4}}. \tag{13b}$$

Subsequently, using the optimized circuit solution from Fig. 12(b) for the equivalent value of the floating capacitor it holds:

$$C_{eq} = \frac{g_{m1}}{g_{m4}} C_g, \tag{14}$$

whereas $g_{m1} = g_{m3}$.

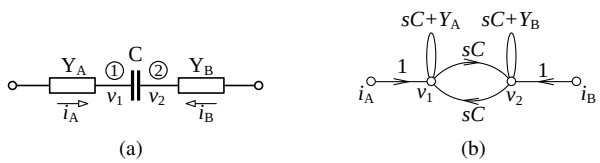

Fig. 10. (a) Floating passive capacitor connected in to an external circuit, (b) corresponding signal flow graph

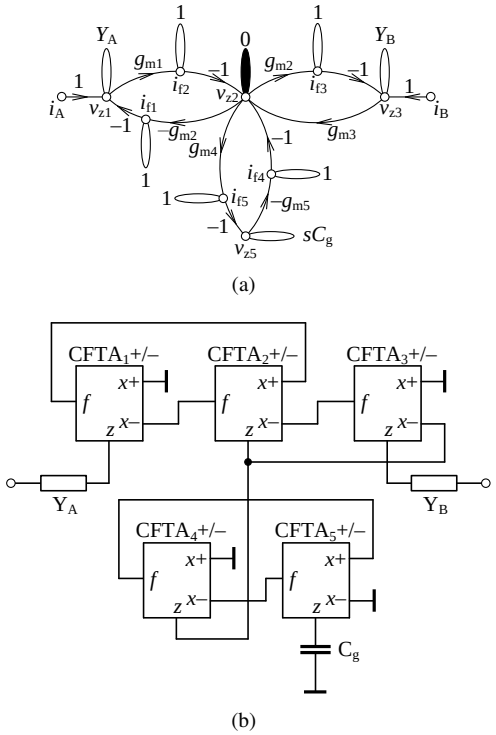

Fig. 11. (a) Signal flow graph of the floating capacitor multiplier using CFTAs, (b) circuit representation

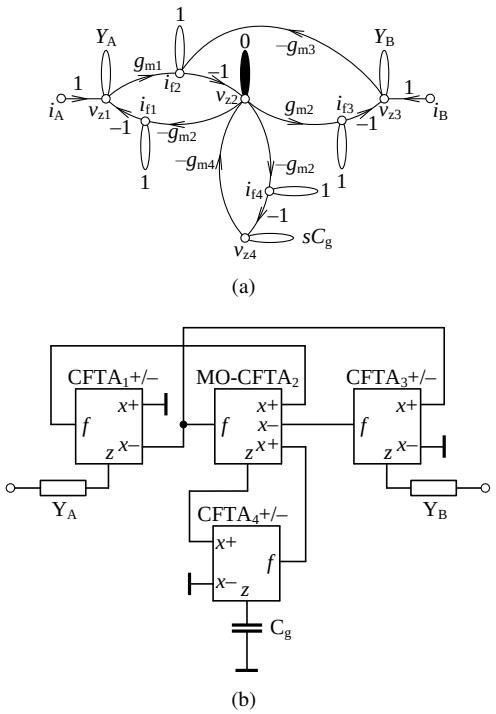

Fig. 12. Optimized solution of the floating capacitor multiplier: (a) signal flow graph, (b) circuit representation

A capacitance multiplier using three CFTAs and one MO-CFTA is also presented in [78]. As shown in Fig. 13(a), in this solution only the OTA part of the two active elements is used. As the current follower part of CFTA_2 and CFTA_4 is

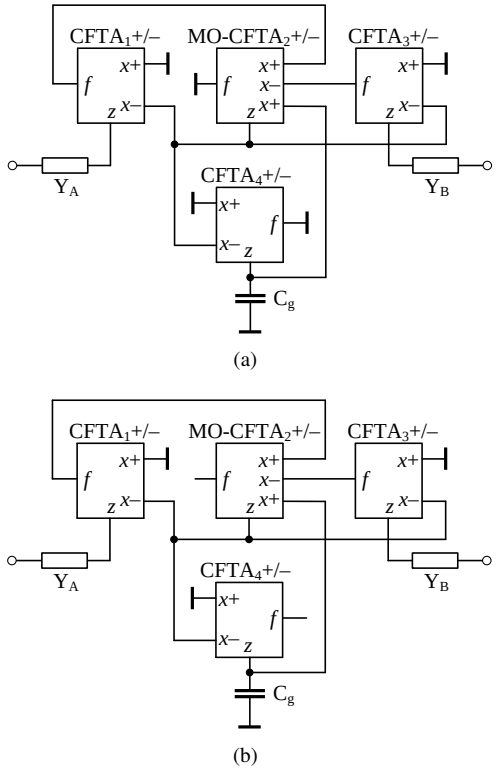

Fig. 13. (a) Floating capacitor multiplier from [78] with grounded f terminals, (b) correct solution with f terminals being floating

not employed the authors connect the current input terminals f to the ground. Such treatment of unused ports of the active element has no influence on the behavior of the function block once ideal active elements are assumed. However, in practice the unused f terminals must be left open to ensure current i_f being zero as shown in Fig. 13(b) or should be used as functional as shown in Fig. 12(b). Note that the notation (polarity) of the x terminals in Fig. 13(a) differ from the notation used in the original solution presented in [78], which is caused by different active element description used in [78].

E. Grounded Capacitor Multiplier

Once employing synthetic inductors or any other synthetic element in the designed structure of a function block that using active elements can be tuned, simple passive capacitors generally to not need to be implemented using active elements. However, for sake of completeness, we also present the grounded capacitor multiplier that can be used if required.

Using signal flow graph, the grounded passive capacitor connected to a circuit can be represented as shown in Fig. 14. The transfer function of the graph can be determined as:

$$\frac{v_1}{i_A} = \frac{1}{sC + Y_A + Y_B}. \tag{15}$$

The signal flow graph of the grounded capacitor multiplier can be derived from the signal flow graph from Fig. 11(a), where the one oriented loop has been omitted as it can be obvious in Fig 15(a). For the transfer function of this graph it

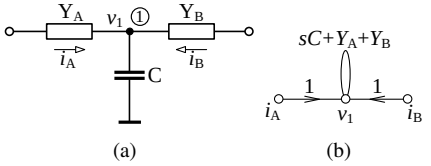

Fig. 14. (a) Grounded passive capacitor connected to a circuit, (b) corresponding signal flow graph

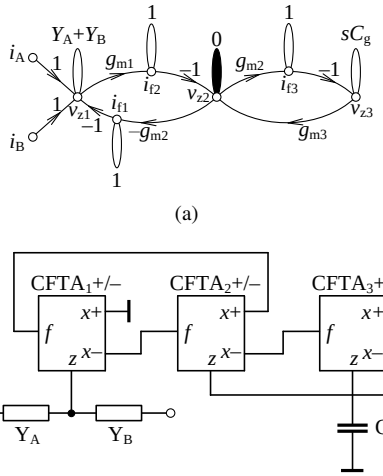

Fig. 15. (a) Signal flow graph of the grounded capacitor multiplier using CFTAs, (b) corresponding circuit representation

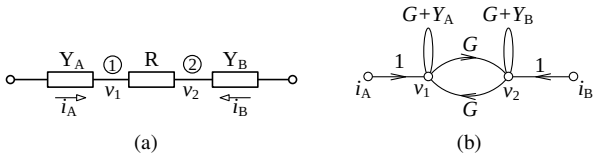

Fig. 16. (a) Floating passive resistor connected to a circuit, (b) corresponding signal flow graph

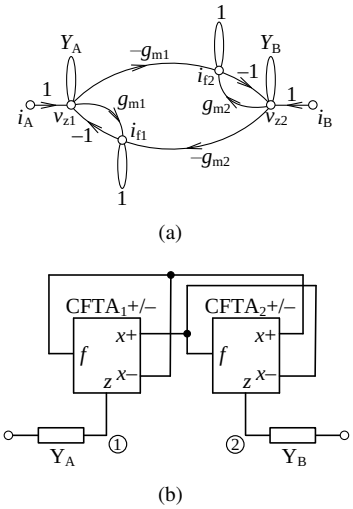

Fig. 17. (a) Signal flow graph of the floating resistor simulator using CFTAs, (b) corresponding circuit representation

holds:

$$\frac{v_{z1}}{i_A} = \frac{g_{m2}g_{m3}}{g_{m1}g_{m2}sC_g + g_{m2}g_{m3}(Y_A + Y_B)}. \tag{16}$$

Comparing (16) and (15) the equivalent value of the grounded capacitor equals to:

$$C_{eq} = \frac{g_{m1}}{g_{m3}}C_g, \tag{17}$$

and the circuit realization of the grounded capacitor multiplier using three CFTAs is shown in Fig. 15(b).

F. Floating Resistor Simulator

Using the CFTAs a floating resistor simulator can also be easily implemented. Following the theoretical background presented in previous sections, the passive resistor R is connected to a circuit represented by general admittances Y_A and Y_B as shown in Fig. 16(a). In the corresponding signal flow graph, the resistor is expressed by its conductivity G (Fig. 16(b)) and the transfer function of this graph is given as:

$$\frac{v_1}{i_B} = \frac{v_2}{i_A} = \frac{G}{GY_A + GY_B + Y_A + Y_B}. \tag{18}$$

Similarly as in case of the floating capacitor multiplier, the signal flow graph of the active resistor simulator cannot be determined directly. To design an active floating resistor simulator two CFTAs are used that in the signal flow graph create three oriented loops as shown in Fig. 17(a). The transfer functions of this graph are:

$$\frac{v_{z2}}{i_A} = \frac{g_{m1}}{g_{m2}Y_A + g_{m1}Y_B + Y_AY_B}, \tag{19a}$$

$$\frac{v_{z1}}{i_B} = \frac{g_{m2}}{g_{m2}Y_A + g_{m1}Y_B + Y_AY_B}. \tag{19b}$$

Comparing (18) and (19) it is evident that it must hold $g_{m1} = g_{m2} = g_m$ and the equivalent value of the floating resistor equals to:

$$R_{eq} = \frac{1}{g_m}. \tag{20}$$

The corresponding representation of the floating resistor simulator is shown in Fig. 17(b).

G. Grounded Resistor Simulator

From the basic passive elements, also the grounded resistor can be implemented using active elements. The representation of a passive resistor connected into a circuit and the corresponding part of the signal flow graph is shown in Fig. 18. The transfer function of the signal flow graph from Fig. 18(b) is given as:

$$\frac{v_1}{i_A} = \frac{1}{G + Y_A + Y_B}. \tag{21}$$

The signal flow graph featuring the same transfer function using active elements can be determined from Fig. 17(a) by proper simplification as shown in Fig. 19(a). This signal flow graph contains only single oriented loop and for its transfer function it holds:

$$\frac{v_z}{i_A} = \frac{1}{Y_A + Y_B + g_m}. \tag{22}$$

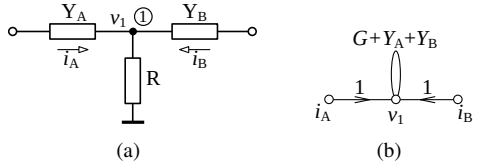

Fig. 18. (a) Grounded passive resistor connected to a circuit, (b) corresponding signal flow graph

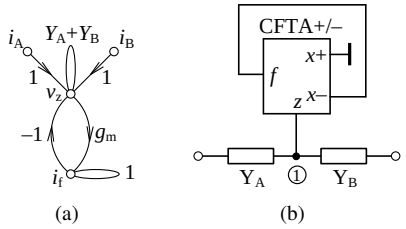

Fig. 19. (a) Signal flow graph of the grounded resistor simulator using CFTA, (b) corresponding circuit representation

The circuit solution using single CFTA is shown in Fig. 19(b) with the equivalent resistance given by (20).

As shown, using the signal flow graph approach it is possible to design active representation of passive elements, both floating and grounded, which can be with advantage used e.g. for frequency filter design that is based on a passive prototype.

IV. Application of Proposed Synthetic Elements

To show the operation and functionality of the proposed synthetic elements described in previous section, some of them are used in simple frequency filters. All the circuits presented in this section were simulated using Spice, whereas the CFTA has been implemented using the UCC-N1B model as shown in Fig. 3(b).

A. Low-pass Frequency Filter

In Fig. 20 the second-order low-pass filter is shown. Here, the floating inductor L is replaced by the corresponding active inductor simulator from Fig. 6(b) and also by active inductor simulator from Fig. 7(b) as shown in Fig. 21.

For the transfer function of the passive prototype from Fig. 20 it holds:

$$K_{pas} = \frac{G}{s^2LCG + sC + G}. \tag{23}$$

and the transfer function of the active filters from Fig. 21 can be determined as:

$$K_{act} = \frac{Gg_{m1}g_{m2}}{s^2C_LCG + sCg_{m1}g_{m2} + Gg_{m2}g_{m3}}, \tag{24}$$

whereas it must hold $g_{m1} = g_{m3}$.

The quality factor Q and angular pole-frequency ω_0 are:

$$Q = G\sqrt{\frac{L}{C}} = G\sqrt{\frac{C_L}{C}\frac{1}{g_{m1}g_{m2}}}, \tag{25a}$$

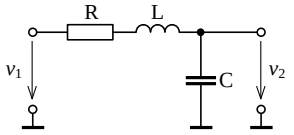

Fig. 20. Passive prototype of low-pass filter

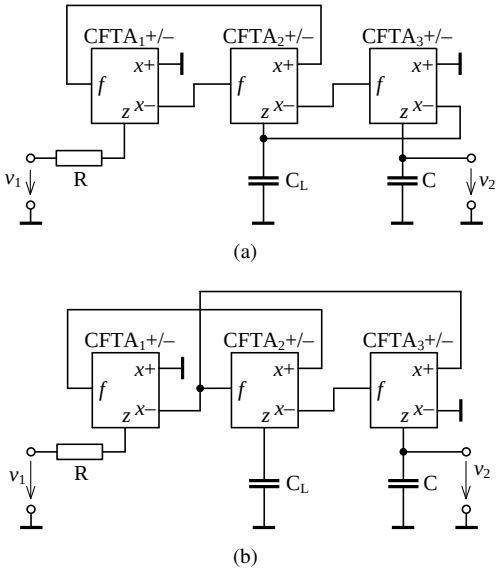

Fig. 21. Active low-pass frequency filter; floating inductor replaced by inductor simulator (a) from Fig. 6(b), (b) from Fig. 7(b)

$$\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{LC}} = \sqrt{\frac{g_{m1}g_{m2}}{C_LC}}. \tag{25b}$$

Using (25), for $Q = 0.707$ and $f_0 = 100$ kHz, the values of passive elements can be determined as: $R = 1$ kΩ, $C = 2.2$ nF and $L = 1$ mH. According to (7), for the active filter we can select $C_L = 2.2$ nF, $g_{m1} = g_{m3} = 1/820$ S and $g_{m2} = 1/560$ S. The simulation results of the transfer function magnitude are shown and compared in Fig. 22. It is evident that the magnitudes are nearly the same hence, the behavior of the floating inductor simulators is correct.

B. High-pass Frequency Filter

The use of the grounded loss-less inductor simulator from Fig. 9(b) is shown on the design of high-pass filter. The passive prototype of the filter is in Fig. 23(a) and the corresponding solution using CFTAs is in Fig. 23(b).

The voltage transfer function of the passive and active high-pass filter are:

$$K_{pas} = \frac{s^2LCG}{s^2LCG + sC + G}, \tag{26a}$$

$$K_{act} = \frac{s^2C_LCG}{s^2C_LCG + sCg_{m1}g_{m2} + Gg_{m1}g_{m2}}, \tag{26b}$$

respectively.

The quality factor Q and the angular pole-frequency ω_0 equal to (25). Hence, for $Q = 0.707$ and $f_0 = 100$ kHz,

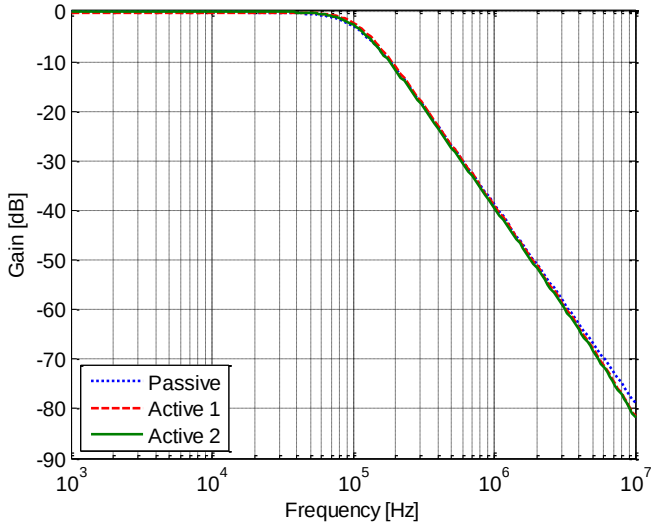

Fig. 22. Magnitude of the low-pass filters from Fig. 20 (Passive), Fig. 21(a) (Active 1) and Fig. 21(b) (Active 2)

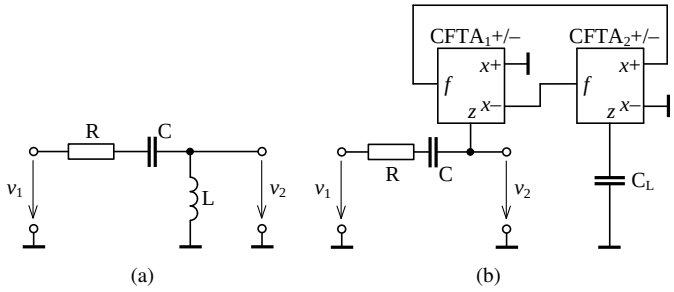

Fig. 23. High-pass frequency filter: (a) passive prototype, (b) filter using inductance simulator from Fig. 9(b)

the values of the passive are $R = 1$ kΩ, $C = 2.2$ nF and $L = 1$ mH. According to (7), for the active filter we can select $C_L = 2.2$ nF, $g_{m1} = g_{m3} = 1/820$ S and $g_{m2} = 1/560$ S. The simulation results of the transfer function magnitude of the passive and active filter solution are shown and compared in Fig. 24. Also here, the magnitudes for the passive and active are nearly the same, which confirms the operability of the inductor simulator. Due to the frequency limitations of the active elements used, which is approx. 30 MHz [33], the gain of the active high-pass filter drops. The affect of the active elements at high frequencies can be also observed in case of the low-pass filter (Fig. 22), however, the higher attenuation in this frequency rage is not detrimental.

C. Band-pass Frequency Filter

To show the operation of the floating capacitor multiplier from Fig. 12(b) it has been used to design a band-pass filter according to the passive prototype from Fig. 25(a). The transfer function of the passive filter is:

$$K_{pas} = \frac{sC}{sLCG + sC + G}. \tag{27}$$

To present the performance only of the capacitor multiplier, the floating inductor has not been replaced by its proper

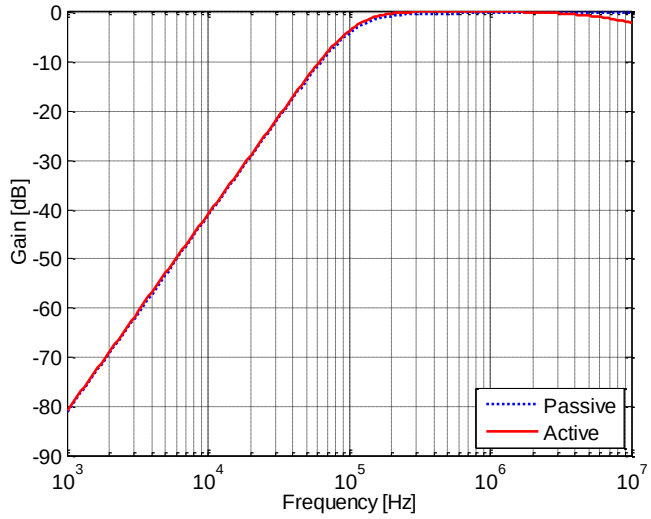

Fig. 24. Magnitude of the high-pass filters from Fig. 23

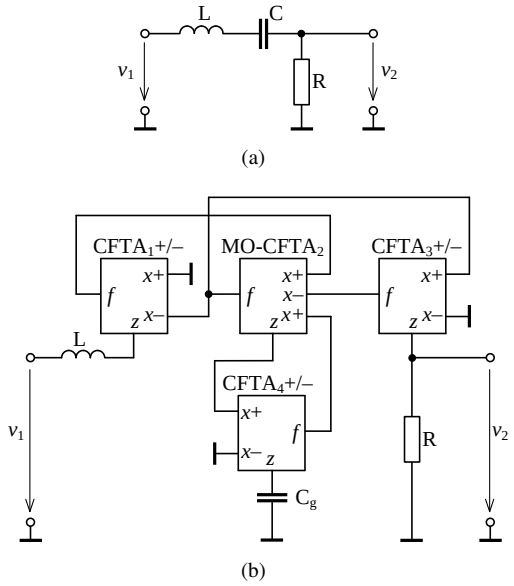

Fig. 25. Band-pass frequency filter: (a) passive prototype, (b) filter using capacitor multiplier from Fig. 12(b)

simulator and the final active band-pass filter is shown in Fig. 25(b). The transfer function of the filter is:

$$K_{act} = \frac{sC_g g_{m1} g_{m2}}{s^2 LC_g G g_{m1} g_{m2} + sC_g g_{m2} g_{m3} + G g_{m2} g_{m4}}. \tag{28}$$

The quality factor Q and the angular pole-frequency ω_0 of the band-pass filters from Fig. 25 are:

$$Q = G\sqrt{\frac{L}{C}} = \frac{G}{g_{m3}}\sqrt{\frac{Lg_{m1}g_{m4}}{C_g}}, \tag{29a}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} = \sqrt{\frac{g_{m4}}{LC_g g_{m1}}}. \tag{29b}$$

Using (29), for $Q = 0.707$ and $f_0 = 100$ kHz, the values of passive elements are $R = 1$ kΩ, $C = 2.2$ nF and $L = 1$ mH. In case of the filter using capacitor multiplier, according to (12)

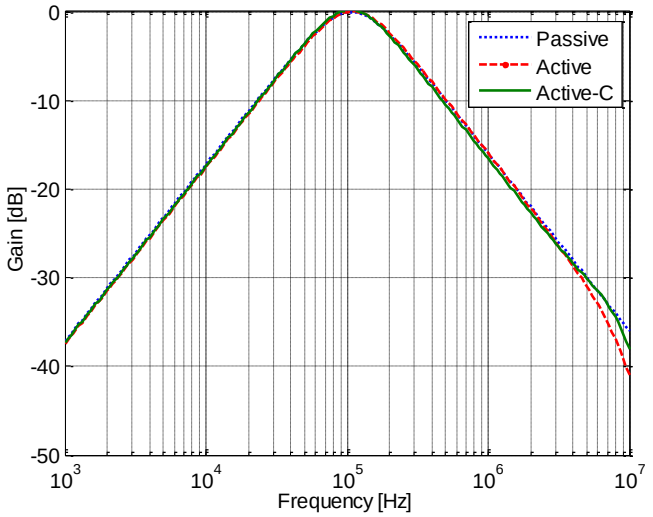

Fig. 26. Magnitude of the band-pass filters from Fig. 25(a) (Passive), from Fig. 25(b) (Active), and from Fig. 27 (Active-C)

the following values selected: $g_{m1} = g_{m2} = g_{m3} = 1$ mS, $g_{m4} = 1/2.2$ mS, and $C_g = 1$ nF to obtain the equivalent value of the floating capacitor C. The simulation results of the band-pass filter are shown in Fig. 26. Based on the results, also in this case it can be stated that the behavior of the proposed floating capacitor multiplier corresponds to the theoretical presumptions. Similarly as in previous cases, at higher frequencies the affect of the active elements can be observed as the attenuation is higher than it is for passive filter. Anyway, in this case such behavior also does not represent a problem.

D. Active-C Band-pass Filter

In previous subsection dealing with the design of band-pass filter, only the floating capacitor has been replaced by its synthetic element (Fig. 25(b)). However, in the passive prototype from Fig. 25(a) (and actually in any other passive circuit), all the passive elements can be replaced by their corresponding active solution presented in section III. Hence, active-C band-pass filter can be proposed as shown in Fig. 27 (see next page) that is described by the following transfer function:

$$K_{active-C} = \frac{sC_g g_{mC1} g_{mL1} g_{mL2}}{s^2 C_L C_g g_{mC1} g_{mR} + sC_g g_{mC1} g_{mL1} g_{mL2} + \\ + g_{mL1} g_{mL2} g_{mR} g_{mC4}}, \tag{30}$$

whereas according to synthetic elements solutions described in section III $g_{mC1} = g_{mC3}$ and $g_{mL1} = g_{mL3}$.

Similarly to the previous cases, the angular pole-frequency ω_0 and quality factor Q of the active-C band pass filter can be defined:

$$\omega_0 = \sqrt{\frac{g_{mL1} g_{mL2} g_{mC4}}{C_L C_g g_{mC1}}}, \tag{31a}$$

$$Q = g_{mR} \sqrt{\frac{C_L}{C_g}} \sqrt{\frac{g_{mC4}}{g_{mC1} g_{mL1} g_{mL2}}}. \tag{31b}$$

Using (31), for $Q = 0.707$ and $f_0 = 100$ kHz, the parameters of the active elements are as follows: $g_{mL1} = g_{mL3} = 1/820$ S, $g_{mL2} = 1/560$ S, $g_{mC1} = g_{mC2} = g_{mC3} = 1$ mS, $g_{mC4} = 1/2.2$ mS, and $g_{mR} = 1$ mS. The values of the two grounded capacitors are $C_L = 2.2$ nF and $C_g = 1$ nF. The simulation results of the transfer function magnitude of the active-C band-pass filter from Fig. 27 are shown in Fig. 26. Here, the behavior of the active-C filter can be compared with the passive filter from Fig. 25(a) and band-pass filter from Fig. 25(b), where only the floating capacitor has been replaced by the corresponding floating capacitor multiplier. As it can be seen, also the properties of active-C filter are satisfactory and agree very well to theoretical presumptions.

V. Conclusion

In this paper, a short overview of application possibilities of the current follower transconductance amplifier (CFTA) active element has been presented. The main attention has been paid to the use of this active element for synthetic element design. Using the signal flow graph approach, except the design of synthetic inductors, also possible realizations of floating and grounded capacitors and resistors were described, where the value of these passive elements can be adjusted by means of active elements parameters. The performance of the selected synthetic elements has been shown on the design of simple frequency filters. The obtained simulation results show that the proposed structures are suitable for active-only frequency filter design, where only grounded capacitors are used.

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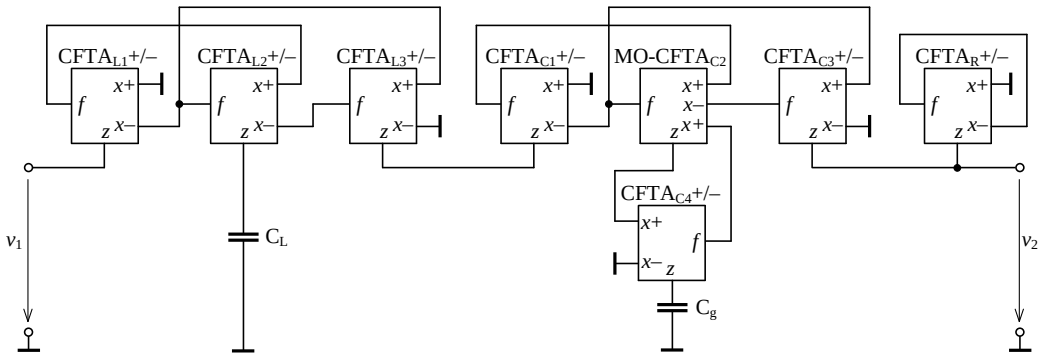

Fig. 27. Active-C band-pass filter based on the passive prototype from Fig. 25(a)

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Gaussian Mixture Density based Analytical Model of Noise Induced Variation in Key Parameter of Electronically Tunable Device

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***Abstract*—In this research, the Gaussian mixture density based analytical model of variation in key parameter of electronically tunable device has been originally proposed. The proposed model is applicable to any electronically tunable device with its tuning variable has been affected by any kind of noise with arbitrary parameters. It has been found from the verification by using different electronically tunable device based empirical distributions and the Kolmogorov-Smirnov tests that this novel model is very accurate. So, it has been found to be a convenient mathematical tool for the analysis and design of various electronically tunable device based circuits.**

***Keywords*—Electronically tunable device, Gaussian mixture density, Multiple order distribution, Non-Gaussian noise.**

I. Introduction

Electronically tunable device for example, operational transconductance amplifier (OTA) [1, 2], current conveyor [3, 4], active resistor [5, 6] and the recently proposed voltage differencing differential difference amplifier (VDDDA) [7] etc., has been found to be applicable in many electronic circuits, for example filters [8]-[12], oscillators [13, 14], phase shifter [15] and full wave rectifier [16]. The key parameter of these devices for example the transconductance, g_m of the OTA etc., has been found to be a function of the tuning variable of the device which can be either voltage or current. Theoretically, perfect tuning which zero variation in key parameter can be obtained is possible. This is because the tuning variable can be assumed to be noise free. Practically, such tuning variable is corrupted by noise. Hence, the perfect tuning mentioned above can never be achieved as noise induced variation in key parameter always exist. This variation is a random process as well as noise and its occurrence is a crucial issue in the analysis and design of any electronically tunable device involved circuit. So, the modeling of the behavior of such variation has been found to be beneficial.

According to this motivation, a novel analytical model of variation in key parameter of electronically tunable device induced by noise in the tuning variable has been proposed in this research. Its derivation has taken multiple time instances into account for completeness without regarding to any specific device and type of tuning variable. This model is applicable to any electronically tunable device either tuned by voltage or current even though such device may contain specific component e.g. Floating Gate MOSFET etc. It is also applicable to device affected by any kind of noise with arbitrary parameters even though such noise may be non-Gaussian [17]-[19], for example, random-telegraph-signal noise [18, 19] etc. This is because this model has been derived based on the renowned Gaussian mixture density [20] which has been used for analytical modeling of many non-Gaussian distributions [21]-[24]. Furthermore, the verification by using different electronically tunable device based empirical distributions as the references and the Kolmogorov-Smirnov tests states that this originally proposed model has been found to be very accurate. Hence, it has been found to be a convenient mathematical tool for the analysis and design of various electronically tunable device involved circuits.

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II. Derivation of The Proposed Model

In this section, derivation of the proposed model will be presented. Obviously, any electronically tunable device is controlled by the tuning variable, u and generate the resulting key parameter $x(u)$ where u can be either voltage or current and $x(u)$ can be any parameter of the device under consideration for example, $x(u) = g_m$ if such device is a transconductor/OTA etc.

As u is corrupted by noise denoted by $n(t)$ in practice, noise induced variation in key parameter, $\Delta x(t)$, unfortunately arises and can be defined as

$$\Delta x(t) = x(u+n(t))-x(u). \quad (1)$$

Since u is extremely small due to the currently renowned low voltage low power (LVLP) design trend, $\Delta x(t)$ can be given by

$$\Delta x(t) = x'(u)n(t), \quad (2)$$

where $x'(u)$ stands for the derivative of $x(u)$ with respected to u. It should be mentioned here that $\Delta x(t)$ is a random process as well as $n(t)$.

In order to analytically model the behavior of $\Delta x(t)$ by taking multiple time instances into account, its multiple order distribution i.e. N^{th} order distribution where $N \geq 1$ has been found to be convenient. So, it is chosen as the proposed model. For its derivation, the N^{th} order distribution of $n(t)$ must be firstly determined. Since $n(t)$ can be either voltage or current as well as u which means that $n(t)$ is an electrical quantity, $n(t)$ is stationary [18, 25] and has been

assumed to be independent, identically distributed. As a result, the N^{th} order distribution of $n(t)$ can be analytically given as follows

$$f_n(n(t_0),t_0;n(t_0+\tau),t_0+\tau,..;n(t_0+(N-1)\tau,t_0+(N-1)\tau)) = \prod_{k=0}^{N-1}[f_n(n(t_0+k\tau),t_0+k\tau)], \quad (3)$$

where t_0 and $f_n(n(t_0+k\tau),t_0+k\tau)$ stand for the initial time instant and the distribution of $n(t_0+k\tau)$ which denotes noise value at any k^{th} time instant. It can be seen that totally N time instances i.e. t_0, $t_0+\tau,\ldots t_0+(N-1)\tau$, have been now taken into consideration. These time instances are equally distributed on time axis because any pair of $t_0+k\tau$ and $t_0+(k+1)\tau$ are obviously separated apart by equal time interval given by τ.

Since $n(t)$ can actually be non-Gaussian with arbitrary parameters, it is appropriate to analytically model the distribution of $n(t_0+k\tau)$ by a Gaussian mixture density as this density can model the distribution of any non-Gaussian random variation. So, $f_n(n(t_0+k\tau),t_0+k\tau)$ can be given by

$$f_n(n(t_0+k\tau),t_0+k\tau) = \sum_{i=1}^{M}[P_i g_{ni}(n(t_0+k\tau),t_0+k\tau)], \quad (4)$$

where $g_{ni}(n(t_0+k\tau),t_0+k\tau)$ denotes the i^{th} Gaussian density component of $n(t_0+k\tau)$ which is a Gaussian density function with μ_{ni} and σ_{ni} as mean and standard deviation, M denotes the size of $f_n(n(t_0+k\tau),t_0+k\tau)$ which can be defined as number of components of $f_n(n(t_0+k\tau),t_0+k\tau)$ and P_i stands for the weight of $g_{ni}(n(t_0+k\tau),t_0+k\tau)$.

With (2)-(4), the above definition of $g_{ni}(n(t_0+k\tau),t_0+k\tau)$ and the principle of random variable transformation which states that if Y is function of X, the distributions of X and Y are related by

$$\int_{-\infty}^{y} g_Y(v)|dv| = \int_{-\infty}^{x(y)} f_X(u)|du|, \quad (5)$$

the proposed model i.e. N^{th} order distribution of $\Delta x(t)$ can be derived as follows

$$f_{\Delta x}(\Delta x(t_0),t_0;\Delta x(t_0+\tau),t_0+\tau,..;\Delta x(t_0+(N-1)\tau,t_0+(N-1)\tau)) = \prod_{k=0}^{N-1}[f_{\Delta x}(\Delta x(t_0+k\tau),t_0+k\tau)], \quad (6)$$

where $f_{\Delta x}(\Delta x(t_0+k\tau),t_0+k\tau)$ denotes the distribution of $\Delta x(t_0+k\tau)$ which is the value of $\Delta x(t)$ at any k^{th} time instant. Of course, $f_{\Delta x}(\Delta x(t_0+k\tau),t_0+k\tau)$ can be given by

$$f_{\Delta x}(\Delta x(t_0+k\tau),t_0+k\tau) = \sum_{i=1}^{M}\left[\frac{P_i\left[|x'(u)|\right]^{-1}}{\sqrt{2\pi}\sigma_{ni}} exp\left[-\frac{[\Delta x(t_0+k\tau)-x'(u)\mu_{ni}]^2}{2[x'(u)]^2\sigma_{ni}^2}\right]\right]. \quad (7)$$

Since $n(t)$ is stationary which means that its parameters such as P_i, μ_{ni} and σ_{ni} etc., are time invariant, and $x'(u)$ is time independent, $\Delta x(t_0+k\tau)$ is identically distributed for any $k \in \{0, 1, 2,\ldots, N\text{-}1\}$. This means that $\Delta x(t)$ is independent, identically distributed and also stationary.

At this point, the proposed model has been already derived. It is applicable to the device affected by noise of any kind with arbitrary parameters because the Gaussian mixture density has been adopted as the basis. It is also applicable to the device affected by Gaussian noise by simply letting $M = 1$ and $P_i = 1$. Moreover, it can be applied to any electronically tunable device with any kind of tuning variable as u can be either voltage or current and $x(u)$ can be any parameter as mentioned above. This point will be illustrated in the subsequent section which the applications of this model to different electronically tunable devices will be demonstrated. Finally, $x'(u)$ can be conveniently determined in a computer aided manner by using various software packages for example, Mathematica, Mathcad and MATLAB etc.

III. Applications of The Model to Different Devices

Firstly, the application of the model to the voltage controlled current source (VCCS) will be illustrated where a VCCS proposed in [26] will be considered. For this VCCS, the tuning variable is the controlling voltage, $V_c = V_a\text{-}V_b$ and the key parameter is the transconductance, $G_m(V_c)$. By applying the model and let $u = V_c$, $x(u) = G_m(V_c)$ and $\Delta x(t_0+k\tau) = \Delta G_m(t_0+k\tau)$ where $\Delta G_m(t_0+k\tau)$ denotes the value at any k^{th} time instant of $\Delta G_m(t)$ which stands for noise induced variation in transconductance of this VCCS, the N^{th} order distribution of $\Delta G_m(t)$ can be analytically given as

$$f_{\Delta G_m}(\Delta G_m(t_0),t_0;\Delta G_m(t_0+\tau),t_0+\tau,..;\Delta G_m(t_0+(N-1)\tau,t_0+(N-1)\tau)) = \prod_{k=0}^{N-1}\left[\sum_{i=1}^{M}\left[\frac{P_i\left[|G'_m(V_c)|\right]^{-1}}{\sqrt{2\pi}\sigma_{n,i}} exp\left[-\frac{[\Delta G_m(t_0+k\tau)-G'_m(V_c)\mu_{ni}]^2}{2[G'_m(V_c)]^2\sigma_{ni}^2}\right]\right]\right]. \quad (8)$$

Secondly the application of the proposed model to the active resistor will be shown. Here, the active resistor realized by using a special kind of MOSFET namely Floating Gate MOSFET (FGMOSFET) proposed in [27] will be considered. For this active resistor, the tuning variable and the key parameter have been found to be the controlling voltage, V_c and the equivalent resistance, $R_{ECH}(V_c)$ respectively. By applying the model and let $u = V_c$, $x(u) = R_{ECH}(V_c)$ and $\Delta x(t_0+k\tau) = \Delta R_{ECH}(t_0+k\tau)$ where $\Delta R_{ECH}(t_0+k\tau)$ denotes the value at any kth time instant of $\Delta R_{ECH}(t)$ which stands for the noise induced variation in the equivalent resistance of this active resistor, the N^{th} order distribution of $\Delta R_{ECH}(t)$ can be analytically found as follows

$$f_{\Delta R_{ECH}}(\Delta R_{ECH}(t_0),t_0;\Delta R_{ECH}(t_0+\tau),t_0+\tau,..;\Delta R_{ECH}(t_0+(N-1)\tau,t_0+(N-1)\tau)) = \prod_{k=0}^{N-1}\left[\sum_{i=1}^{M}\left[\frac{P_i\left[|R'_{ECH}(V_c)|\right]^{-1}}{\sqrt{2\pi}\sigma_{n,i}} exp\left[-\frac{[\Delta x(t_0+k\tau)-R'_{ECH}(V_c)\mu_{ni}]^2}{2[R'_{ECH}(V_c)]^2\sigma_{ni}^2}\right]\right]\right]. \quad (9)$$

Next, the application of the model to the current conveyor will be illustrated where the 2nd generation current controlled current conveyor (CCCII) proposed in [3] has been chosen for consideration. For this current conveyor, the tuning variable is the biasing current, I_o and the key parameter is the parasitic resistance at port X of the CCCII,

$R_X(I_o)$. Similarly to the previous cases, the N^{th} order distribution of noise induced variation in parasitic resistance, $\Delta R_X(t)$ can be determined by applying the model. In order to do so, we must let $u = I_o$, $x(u) = R_X(I_o)$ and $\Delta x(t_0+k\tau)=\Delta R_X(t_0+k\tau)$ where $\Delta R_X(t_0+k\tau)$ denotes the value at any k^{th} time instant of $\Delta R_X(t)$. As a result, the N^{th} order distribution of $\Delta R_X(t)$ can be analytically given by

$$f_{\Delta R_X}(\Delta R_X(t_0), t_0; \Delta R_X(t_0+\tau), t_0+\tau, ..; \Delta R_X(t_0+(N-1)\tau, t_0+(N-1)\tau)) = \prod_{k=0}^{N-1}\left[\sum_{i=1}^{M}\left[\frac{P_i\left[\left|R_X'(I_o)\right|\right]^{-1}}{\sqrt{2\pi}\sigma_{n,i}} exp\left[-\frac{\left[\Delta x(t_0+k\tau)-R_X'(I_o)\mu_{ni}\right]^2}{2\left[R_X'(I_o)\right]^2\sigma_{ni}^2}\right]\right]\right]. \quad (10)$$

Finally, the application of this model to the VDDDA will be shown where the VDDDA proposed in [7] will be considered. In this case, the tuning variable is the control current, I_B and the key parameter is the transconductance, $g_m(I_B)$. Similarly to the previous cases, the N^{th} order distribution of noise induced variation in the transconductance, $\Delta g_m(t)$ can be analytically determined by applying the model. In order to do so, we must let $u = I_B$, $x(u) = g_m(I_B)$ and $\Delta x(t_0+k\tau)=\Delta g_m(t_0+k\tau)$ where $\Delta g_m(t_0+k\tau)$ denotes the value at any k^{th} time instant of $\Delta g_m(t)$. As a result, the N^{th} order distribution of $\Delta g_m(t)$ can be analytically given as follows

$$f_{\Delta g_m}(\Delta g_m(t_0), t_0; \Delta g_m(t_0+\tau), t_0+\tau, ..; \Delta g_m(t_0+(N-1)\tau, t_0+(N-1)\tau)) = \prod_{k=0}^{N-1}\left[\sum_{i=1}^{M}\left[\frac{P_i\left[\left|g_m'(I_B)\right|\right]^{-1}}{\sqrt{2\pi}\sigma_{n,i}} exp\left[-\frac{\left[\Delta x(t_0+k\tau)-g_m'(I_B)\mu_{ni}\right]^2}{2\left[g_m'(I_B)\right]^2\sigma_{ni}^2}\right]\right]\right]. \quad (11)$$

At this point, it can be seen that the distributions of the variations in key parameters of different electronically tunable devices i.e. VCCS, active resistor current conveyor and VDDDA can be analytically obtained in the similar manner by applying the proposed model. Apart from these devices, this model can be applied to other electronically tunable devices as well for example, OPAMP, active inductor [13], Operational Transresistance Amplifier (OTRA) [14, 28], Current Difference Transconductance Amplifier (CDTA) [16], Current Differencing Buffered Amplifier (CDBA) [29], Voltage Differencing Transconductance Amplifier (VDTA) [30], Voltage Differencing Buffered Amplifier (VDBA) [31], Voltage Differencing Current Conveyor (VDCC) [32] and active transformer [33] etc. This is because it has been derived regardless to any specific device. Furthermore it is also applicable to those devices based on any special component apart from the FGMOSFET such as FinFET [34] and Carbon nanotube FET (CNTFET) [35] etc., since it has been derived regardless to any specific component.

IV. The Model Verification

In this section, the verification of the proposed model will be addressed. It should be mentioned here that the 0.25μm CMOS process technology of TSMC has been adopted as the verification basis. Since $\Delta x(t)$ is stationary which means that its behavior is time independent, it is sufficient to perform the verification at an arbitrary instant since the obtained results are always valid. Such verification has been performed based on the VCCS, active resistor, current conveyor (CCCII) and VDDDA proposed in [26], [27], [3] and [7] respectively. It has been assumed the tuning variable of the active resistor is corrupted by the impulse noise (random telegraph noise) [18, 19] where those of the VCCS and the current conveyor are respectively corrupted by the student-t noise and the Rayleigh noise which can occur since noise can be non-Gaussian [17]-[19]. On the other hand, the tuning variable of the VDDDA has been assumed to be corrupted by the Gaussian noise in in order to verify the accuracy of the model when applied to the device affected by such noise.

For the verification in the qualitative manner, the analytically determined distributions of $\Delta G_m(t)$, $\Delta R_{ECH}(t)$, $\Delta R_x(t)$ and $\Delta g_m(t)$ obtained by using the proposed model have been comparatively plotted against their corresponding references which are the electronically tunable device based empirical distributions obtained by using the 0.25μm level SPICE BSIM3v3 based Monte-Carlo simulations with parameters provided by MOSIS. On the other hand, the verification in the quantitative manner has been performed via the KS-tests [36, 37] of these analytically obtained distributions. The KS-test has been chosen due to its simpler statistic compared to the others and its capability to fit non-Gaussian distributions [37]. In general, the KS-test of any distribution can be performed by comparing its statistic, *KS* to the critical value, *c* where it can be stated that the distribution under test fits the empirical distribution at any certainly specified confidence level if and only if $KS \le c$. Mathematically, *KS* can be given by

$$KS = \max_x\left\{\left|\int_{-\infty}^{x} f_X'(u)du\right| - \left|\int_{-\infty}^{x} f_X(u)du\right|\right\}, \quad (12)$$

where $f_X(x)$ and $f_X'(x)$ denote the distribution under test and the empirical distribution respectively.

Since confidence level of the test is chosen to be 99%, *c* can be given by [36]

$$c = \frac{1.63}{\sqrt{n}}, \quad (13)$$

where *n* denotes the number of runs of each Monte-Carlo simulation. It should be mentioned here that $c = 0.02976$ because $n = 3000$. At this point, the model verification based on VCCS, active resistor, current conveyor and VDDDA will be subsequently presented.

A. The verification based on the VCCS affected by the student-t noise

In this subsection, the verification based on the VCCS with V_c corrupted by the student-t noise, will be presented. Since it is assumed that the equivalent mean and equivalent standard deviation of noise are 0 V and 1.4239 nV respectively, its distribution can be analytically modeled by using a Gaussian mixture density. By letting $M = 5$ and applying the maximum likelihood parameter estimation, it has been found that $P_1 = 0.31$, $P_2 = 0.005$, $P_3 = 0.68$, $P_4 = P_5$

= 0.0025, $\mu_{n1} = \mu_{n2} = \mu_{n3} = \mu_{n4} = \mu_{n5} = 0$ V, $\sigma_{n1} = \sqrt{2}$ nV, $\sigma_{n2} = \sqrt{20}$ nV, $\sigma_{n3} = \sqrt{1.5}$ nV, $\sigma_{n4} = \sqrt{15}$ nV and $\sigma_{n5} = \sqrt{10}$ nV. For the verification in the qualitative sense, the analytically determined distribution of $\Delta G_m(t)$ has been comparatively plotted against its reference which is the VCCS based empirical distribution, as shown in Fig.1 where the horizontal axis shows that the unit of $\Delta G_m(t)$ is the percentage of the nominal $G_m(V_c)$ which V_c is noise free. From Fig.1, a strong agreement between the analytically determined distribution and its reference can be observed.

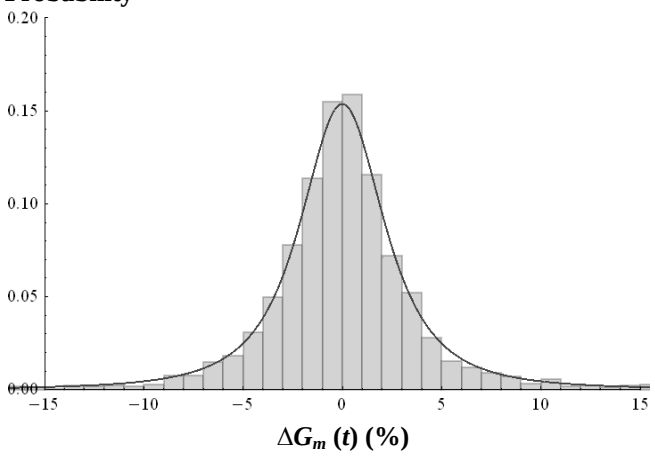

Fig.1. Analytically determined distribution of $\Delta G_m(t)$ (line) v.s. The VCCS based empirical distrubution (histogram)

For the verification in the quantitative manner, the KS-test of the analytically determined distribution of $\Delta G_m(t)$ has been performed. In this case, such distribution serves as $f_X(x)$ where the VCCS based empirical distribution serves as $f_X^{'}(x)$. By using (12), it has been found that KS = 0.00195 which satisfies $KS \le c$ as c = 0.02976. This means that the analytically determined distribution fits its reference with 99% confidence. Since the results of the verification in both qualitative and quantitative manners have been found to be very pleasant, the accuracy of the proposed model has been now verified.

Furthermore, the analytically determined distribution of $\Delta G_m(t)$ shows that $\Delta G_m(t)$ has a student-t distribution with zero equivalent mean as the VCCS based empirical distribution does. $\Delta G_m(t)$ has zero equivalent mean because V_c is corrupted by noise with zero equivalent mean. The analytically determined distribution and the empirical distribution give the equivalent standard deviations of 7.27% and 7.06% respectively. It can be seen that these standard deviations are very close to each other. This also verifies the accuracy of the proposed model.

B. The verification based on the active resistor affected by the impulse noise

In this subsection, the verification based on the active resistor with V_c corrupted by the impulse noise will be presented. Here, it has been assumed that such impulse noise has two levels.

Since the distribution of any two level impulse random signal, $s(t)$ which the value of each level is deterministic, can be given by

$$h(s(t),t) = \begin{cases} P & ;s(t) = S_1 \\ 1-P & ;s(t) = S_2 \\ 0 & ;(s(t) \neq S_1) \wedge (s(t) \neq S_2) \end{cases}, \quad (14)$$

where S_1 and S_2 are certain possible deterministic values of $s(t)$, the distribution of two level impulse noise can be analytically modeled by using Gaussian mixture density with M = 2, $P_1 = P$ and P_2 = 1-P. Since the equivalent mean and equivalent standard deviation of such noise are assumed to be 80 nV and 89.445 nV respectively, it has been found that P_1 = 0.5, P_2 = 0.5, μ_{n1} = 40 nV, μ_{n2} = 120 nV, $\sigma_{n1} = \sqrt{0.6}$ nV and $\sigma_{n2} = \sqrt{0.4}$ nV by using the maximum likelihood parameter estimation.

As the verification in the qualitative manner, the analytically determined distribution of $\Delta R_{ECH}(t)$ has been comparatively plotted against its reference i.e. the active resistor based empirical distribution as shown in Fig.2 where the horizontal axis shows that the unit of $\Delta R_{ECH}(t)$ is the percentage of the nominal $R_{ECH}(V_c)$ which V_c is noise free. From Fig.2, a strong agreement between the analytical distribution and its reference can be observed.

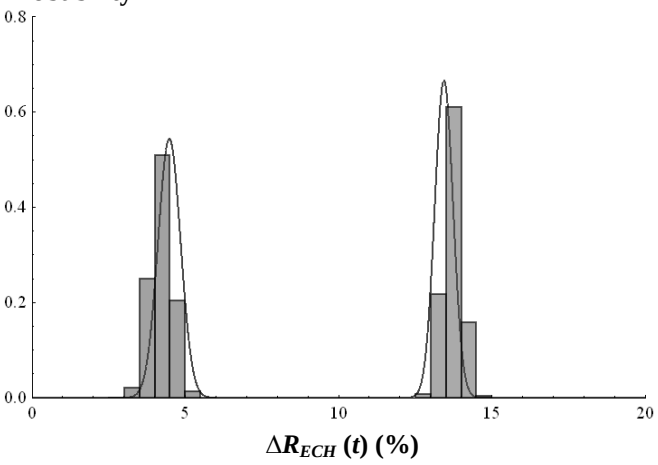

Fig.2. Analytically determined distribution of $\Delta R_{ECH}(t)$ (line) v.s. The active resistor based empirical distribution (histogram)

As the verification in the quantitative sense, the KS-test of the analytically determined distribution of $\Delta R_{ECH}(t)$ has been performed where such distribution serves as $f_X(x)$ and the active resistor based empirical distribution serves as $f_X^{'}(x)$ in this case. By using (12), it has been found that KS = 0.018 which also satisfies $KS \le c$ as c = 0.02976. This means that the analytically determined distribution fits its reference with 99% confidence. As the results of the verification in both qualitative and quantitative manners have been found to be very pleasant, the proposed model has been found to be accurate.

Moreover, both analytically determined distribution of $\Delta R_{ECH}(t)$ and active resistor based empirical distribution show that $\Delta R_{ECH}(t)$ has a Gaussian mixture distribution with two levels. The analytically determined distribution gives the equivalent mean and standard deviation of 8.96% and 10.02% respectively. On the other hand, the equivalent mean and standard deviation obtained from the empirical distribution can be respectively given by 8.42% and 9.42%.

It can be seen that these sets of parameters are very close to each other. This also verifies the accuracy of the model.

C. The verification based on the current conveyor affected by the Rayleigh noise

In this subsection, the verification based on the current conveyor i.e. CCCII with I_o corrupted by the Rayleigh noise will be presented. It has been assumed that the equivalent mean and equivalent standard deviation of noise are given by 60.553 nA and 31.623 nA respectively. For the verification in the qualitative manner, the analytically determined distribution of $\Delta R_X(t)$ has been comparatively plotted against its reference i.e. the current conveyor based empirical distribution as shown in Fig.3 where the unit of $\Delta R_X(t)$ is the percentage of the nominal $R_X(I_o)$ which I_o is noise free. From Fig.3, a strong agreement between the analytically determined distribution and its reference can also be seen.

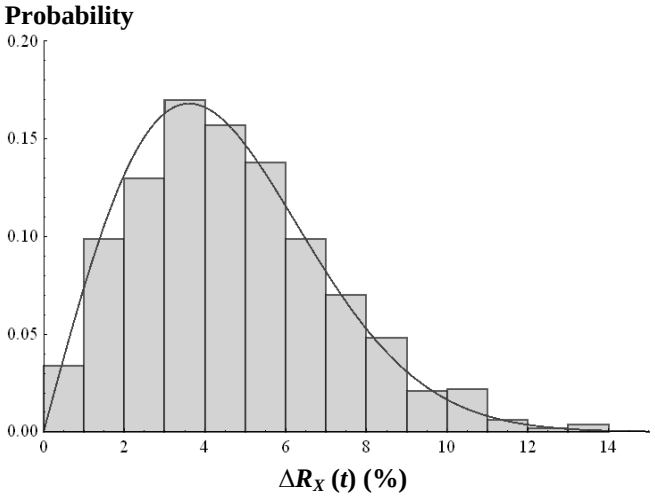

Fig.3. Analytically determined distribution of $\Delta R_X(t)$ (line) v.s. The current conveyor based empirical distribution (histogram)

As the verification in the quantitative sense, the KS-test of the analytically determined distribution of $\Delta R_X(t)$ has been performed. Now, such distribution and the current conveyor based empirical distribution serves as $f_X(x)$ and $f_X^{'}(x)$ respectively. By using (12), it has been found that KS = 0.022 which also satisfies $KS \leq c$ as c = 0.02976. This means that the analytically determined distribution fits its reference with 99% confidence. At this point, the accuracy of the proposed model has been now verified according to the soundness of the results of verification in both senses mentioned above.

Moreover, both analytically determined distribution of $\Delta R_X(t)$ and active resistor based empirical distribution show that $\Delta R_X(t)$ has a Rayleigh distribution. The analytically determined distribution gives the equivalent mean and standard deviation of 4.523% and 2.364% respectively. On the other hand, the equivalent mean and standard deviation obtained from the empirical distribution can be respectively given by 4.72% and 2.465%. It can be seen that these sets of statistical parameters are very close to each other. This alternatively verifies the accuracy of the proposed model.

D.The verification based on the VDDDA affected by the Gaussian noise

Now, the verification based on the VDDDA with I_B corrupted by the Gaussian noise will be presented. It has been assumed that mean and standard deviation of such noise are 0 V and 1.1559 nV respectively. For the verification in the qualitative sense, the analytically determined distribution of $\Delta g_m(t)$ has been comparatively plotted against its reference which is the VDDDA based empirical distribution, as shown in Fig.4 where the unit of $\Delta g_m(t)$ is the percentage of the nominal $g_m(I_B)$ which I_B is noise free. From Fig.4, a strong agreement between the analytical distribution and its reference can be observed.

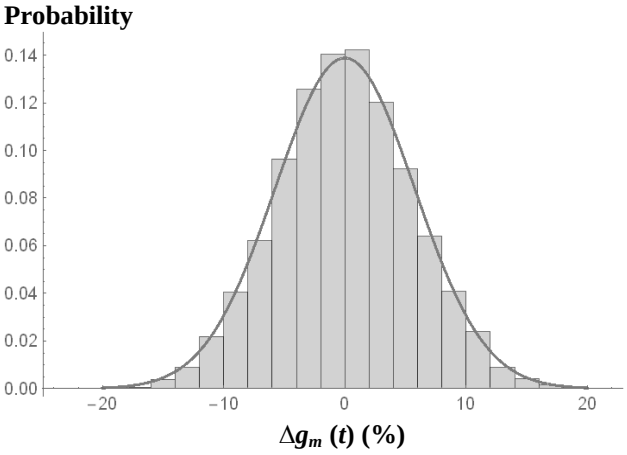

Fig.4. Analytically determined distribution of $\Delta g_m(t)$ (line) v.s. The VDDDA based empirical distribution (histogram)

For the verification in a quantitative manner, the KS-test of the analytical distribution of $\Delta g_m(t)$ has been performed where such distribution serves as $f_X(x)$ and the VDDDA based empirical reference serves as $f_X^{'}(x)$. By using (12), it has been found that KS = 0.00225 which satisfies $KS \leq c$ as c = 0.02976. This means that the analytically determined distribution fits its reference with 99% confidence. So, the proposed model has been found to be very accurate according to the soundness of the results of verification in both manners.

Furthermore, the analytically determined distribution of $\Delta g_m(t)$ states that $\Delta g_m(t)$ has a zero mean Gaussian distribution as the VDDDA based empirical distribution does. Such distribution of $\Delta g_m(t)$ is obtained because I_B is corrupted by a zero mean Gaussian noise. The analytically determined distribution and its reference give the standard deviations of 5.75% and 5.53% respectively which are very close to each other. This also verifies the accuracy of the proposed model.

V. CONCLUSION

The Gaussian mixture density based analytical model of the variation in key parameter of any electronically tunable device induced by noise in tuning voltage/current which can be any kind with arbitrary parameters, has been originally derived in this research. Its applications to different electronically tunable devices have been demonstrated. The verification performed by using different electronically

tunable device based empirical distributions as the references and the 99% confidence level KS-tests states that this model is very accurate. Hence, it has been found to be beneficial to the analysis and design of various circuits involving electronically tunable devices.

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