

Design and FPGA Implementation of Variable Cutoff Frequency Filter based on Continuously Variable Fractional Delay Structure and Interpolation Technique

Sumedh Dhabu and A. P. Vinod

Abstract—This paper presents the design and FPGA implementation of interpolated continuously variable fractional delay structure based filter (ICVFD filter) with fine control over the cutoff frequency. In the ICVFD filter, each unit delay of the prototype lowpass filter is replaced by a continuously variable fractional delay (CVFD) element proposed in this paper. The CVFD element requires the same number of multiplications as that of the second-order fractional delay structure used in the existing fractional delay structure based variable filter (FDS based filter), however it provides fractional delays corresponding to the higher-order fractional delay structures. Hence, the proposed ICVFD filter provides wider cutoff frequency range compared to the FDS based filter. The ICVFD filter is also capable of providing variable bandpass and highpass responses. We use two-stage approach for the FPGA implementation of the ICVFD filter. First, we use pipelining stages to shorten the critical path and improve the operating frequency. Then, we make use of specific hardware resource, i.e. RAM-based Shift Register (SRL) to further improve the operating frequency and resource usage.

Keywords—FPGA implementation, fractional delay structure based filter, reconfigurable digital filter, variable cutoff frequency filter.

I. INTRODUCTION

Variable finite impulse response (FIR) filters (FIR filters whose frequency response can be changed based on the desired specifications) are widely used in digital communications. The frequency response of an FIR filter can be changed by completely changing its coefficients or by modifying the impulse response using various operations. In the programmable digital filters [1]-[4], the desired frequency responses are obtained by updating all the filter coefficients which are stored in the memory. This is a very simple approach, and in general, the variable coefficient filters are optimum in a sense that the filter length for the particular frequency response specifications is the minimum. However, when the frequency response of the filter needs to be changed frequently, large number of memory access operations make updating routines of these filters time consuming. Other approaches proposed in the literature [5]-[12] modify the impulse response of the fixed-coefficient

prototype filter by controlling fewer parameters, without the need of updating all the filter coefficients.

In the interpolation approach [5], each delay of the fixed-coefficient filter structure is replaced by M delays to obtain a multiband response and then the desired band is extracted using a masking filter. In the coefficient decimation method (CDM) [6], the impulse response of the fixed-coefficient filter is modified by retaining every D^{th} coefficient of the filter and either replacing the remaining coefficients by zeros or by completely discarding them. The cutoff frequency of the coefficient decimated filter can be an integer multiple of the cutoff frequency of the prototype filter. Even though the interpolation and CDM techniques are simple to implement (as they need only multiplexers to vary M or D) and the filters realized using [5] and [6] have low complexities, they provide only coarse control over the cutoff frequency due to the discrete nature of the controlling parameters (M and D).

A very fine control over the cutoff frequency of the filter can be obtained at the cost of increase in the complexity of the filter structure. In [7], an all-pass transformation based variable filter is realized by replacing the unit delay of the prototype filter by the first- or second-order all-pass structure. Even though the prototype filter in [7] is a linear-phase filter, the resultant filter is not a linear-phase filter due to the use of all-pass transformation. As opposed to the all-pass transformations, the frequency transformation based filters preserve the linear-phase property of the prototype filter [8]. However, the transition bandwidth of the frequency transformation based filter can be significantly wider than that of the prototype filter. The spectral parameter approximation (SPA) technique [9], [10] makes use of weighted combination of the fixed-coefficient FIR sub-filters to generate the desired frequency response and provides absolute control over the cutoff frequency of the filter in the desired range. However, the complexity of the SPA technique is higher than all the other approaches. In [11], a set of fixed-coefficient filters is used where each filter takes care of only specific part of the variable frequency regions. This technique requires large number of filters when the desired cutoff frequency range is large.

In [12], the unit delay element of the filter is replaced by the fractional delay structure (FDS). In this FDS based filter [12], a single parameter (d) varies the value of the fractional delay; thereby modifying the sample values and the length of the impulse response of the filter, resulting in a variable

digital filter with fine control over the cutoff frequency. A second-order modified Farrow structure [13] is used to replace the unit delay of the prototype filter in [12]. Therefore, cutoff frequency of the filter varies according to the value of the fractional delay ($1 \leq 1+d < 2$). However, the cutoff frequency, f_c , can be varied only in the limited range given by $f_{c_mod}/2 < f_c \leq f_{c_mod} \leq 0.2$ where f_{c_mod} is the cutoff frequency of the prototype filter. (Please note that all the frequency values mentioned in this paper are normalized with respect to half the sampling frequency, i.e. π .) It is observed that the FDS based filter provides unity magnitude response and constant phase response only for the cutoff frequencies in the lower range of the Nyquist band [12]. The second-order modified Farrow structure can provide the unity magnitude response and constant phase response only for the low frequencies (approximately up to 0.2) [13, 14], which results in degradation in the response of the FDS based filter for higher cutoff frequencies. Therefore, the maximum cutoff frequency obtained from the FDS based filter can be approximately 0.2.

In [12], CDM is used to increase the cutoff frequency range of the FDS based filter. Therefore, the cutoff frequency range can be $f_{c_mod}/2 < f_c \leq 2f_{c_mod} \leq 0.2$. However, the prototype filter needs to be overdesigned, i.e. its order should be increased, in order to compensate for the passband ripple, stopband attenuation and transition bandwidth degradation which is inherent to the CDM.

In this paper we present the design and FPGA implementation of modified fractional delay structure based filter to overcome the lower limit on the cutoff frequency of the FDS based filter. The proposed interpolated continuously variable fractional delay structure based filter (ICVFD filter) uses the continuously variable fractional delay (CVFD) structure. This CVFD element provides wider delay range, equivalent to the delay range obtained from the higher-order fractional delay structure, without increasing the number of multiplications required. The ICVFD filter uses the CVFD element and the interpolation technique and provides a *continuous* control over the cutoff frequency of the filter. The ICVFD filter is capable of producing variable lowpass, bandpass and highpass filter responses.

The rest of the paper is organized as follows. Section II presents the details of the CVFD element and the ICVFD filter. A design example and comparison of the ICVFD filter with the existing variable filters is also presented in Section II. Section III presents the details of pipelining and use of specific hardware resources for implementing the ICVFD filter. The FPGA implementation results are presented in Section IV. Finally Section V concludes this paper.

II. PROPOSED ICVFD FILTER

A. CVFD Element

The CVFD element provides the delay,

$$D_p = p + 1 + d \quad (1)$$

where the fractional delay equal to $1+d$ is provided by the second-order modified Farrow structure, and the variable number of p unit delays are added using a multiplexer, as shown in Fig. 1. The fractional delay range of this CVFD element can be changed online as follows. For $p = 0$, the

fractional delay range is $1 \leq D_p < 2$, whereas the fractional delay range changes to $2 \leq D_p < 3$ for $p = 1$, and so on. For the other fractional delay structures, the multiplication complexity of the fractional delay structure (i.e. the number of multiplications required) increases with the range of fractional delay to be obtained [13-15]. However, the CVFD element provides the fractional delay same as the higher-order fractional delay structure, at the same multiplication complexity as that of the second-order fractional delay structure. Further, as the second-order modified Farrow structure has the least multiplication complexity among the second-order fractional delay structures, the proposed CVFD element is capable of providing the fractional delay equivalent to the fractional delay provided by higher-order fractional delay structures for the least multiplication complexity possible.

Another advantage of the CVFD element is that the fractional delay range can be changed online. For the modified Farrow structure based fractional delay structures [13], only the value of fractional delay can be changed online, and not the fractional delay range. The fractional delay range depends on the order of the structure, and therefore, the structures of different orders are required to change the fractional delay range. The second-order fractional delay structures can provide the fractional delay range of 1 to 2 only, and the third-order fractional delay structures can provide the delay range of 2 to 3 only. Hence, these are not suitable when the fractional delay range needs to be changed in the FDS based filter.

Similar to the proposed CVFD element, the fractional delay structure proposed in [15] is capable of changing the fractional delay range on-the-fly. However, as mentioned previously, multiplication complexity of the CVFD element is less than that of the fractional delay structure in [15]. It may be possible to use fractional delay structures based on other implementation strategies [14] which can change the fractional delay range online, but the multiplication complexity of such structures is higher, and therefore the multiplication complexity of the FDS based filter increases. In the CVFD element, the fractional delay range can be changed online without any additional multiplication complexity for the FDS based filter.

B. ICVFD Filter

The proposed ICVFD filter is the combination of the FDS based filter in which the CVFD element replaces the unit delay of the filter and the interpolation technique as shown in Fig. 2. Note that the input signal is fed to the filter and not to the CVFD element. The CVFD element is just used to replace the unit delay of the filter. The interpolation of the CVFD element by factor M results in a delay, D_c , given by

$$D_c = p + (1+d) \times M \quad (2)$$

Therefore, the cutoff frequency and the transition bandwidth of the ICVFD filter, f_{c_ICVFD} and tbw_{ICVFD} respectively, are given by

$$f_{c_ICVFD} = f_{c_mod} / D_c \quad (3)$$

$$tbw_{ICVFD} = tbw_{mod} / D_c \quad (4)$$

where f_{c_mod} is the cutoff frequency of the prototype (modal) filter and tbw_{mod} is the transition bandwidth of the prototype filter.

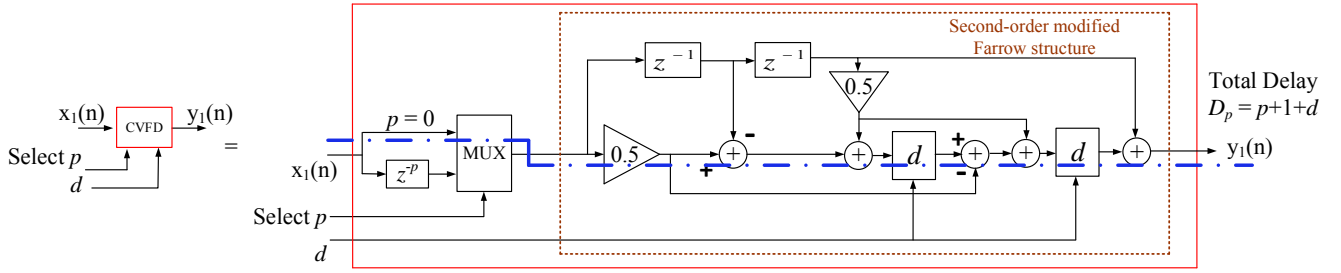


Fig. 1. CVFD element.

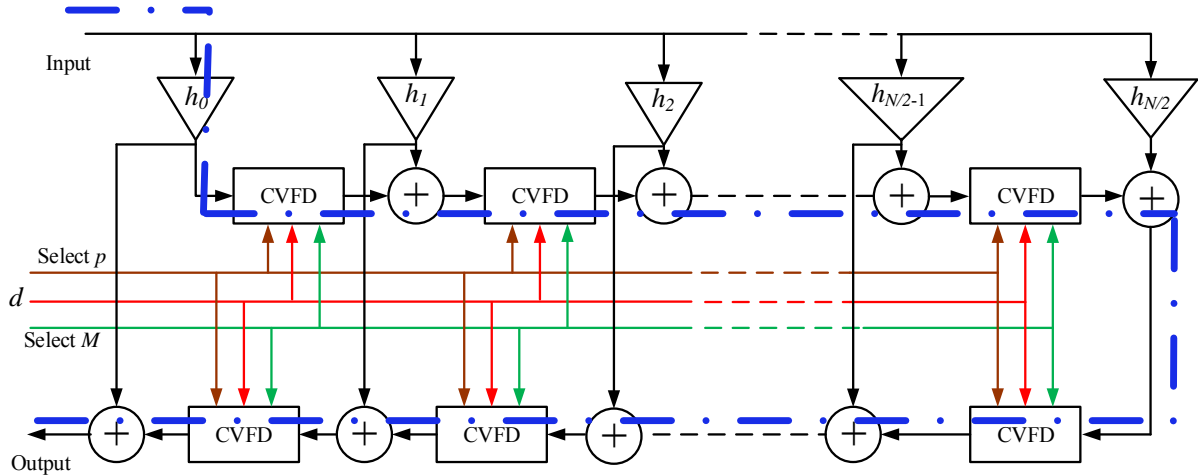


Fig. 2. Modal filter structure of the proposed ICVFD filter.

C. Variable Filter Responses obtained from ICVFD Filter

1. When $p = 0$

In the ICVFD filter, the cutoff frequency of the filter is controlled using three parameters viz. d , M and p . When $p = 0$ and $M = 1$, the ICVFD filter is equivalent to the FDS based filter. When $p = 0$ and M is varied, the ICVFD filter produces variable lowpass, bandpass and highpass filter responses. The cutoff frequencies of the bands in the multiband response are given by $f_{Ai} \pm f_{c_ICVFD}$, where f_{c_ICVFD} is defined in (3), with parameter $p = 0$ for the fractional delay D_c , i.e. the cutoff frequencies are $f_{Ai} \pm \{f_{c_mod}/(1+d)\}/M$, where f_{Ai} are the center frequencies of the bands in the multiband response given by,

$$f_{Ai} = 2i / M, \quad i = 0 \text{ to } M - \lceil M / 2 \rceil \quad (5)$$

The transition bandwidth of the bands in the multiband response is given by (4). The desired band can be extracted by using a suitable masking filter.

The variable bandwidth and variable center frequency responses obtained for the restricted range of D_c , i.e. when $p = 0$ are shown in Fig. 3. The magnitude responses obtained for $f_{c_mod} = 0.2$, $M = \{1, 2, 3, 4\}$ and $d = \{0, 0.1, 0.3, 0.7\}$ are shown in this figure. Four distinct colors and line styles are used to distinguish between the responses obtained for different values of M . The four responses of same color and line style (i.e. the responses obtained for the same value of M) correspond to the four values of the parameter d . Only 4 values of the parameter d are used in this illustration, so as to maintain the clarity of the figure and also to simultaneously show the fine variations in the cutoff frequency. The cropped version of the responses are also shown as inset to illustrate that no degradation occurs in the passband ripple of the ICVFD filter compared to the passband ripple of the modal filter. This is in contrast to the

FDS based filter where magnitude response for all the frequencies above 0.2 is distorted, even though they fall in the passband of the FDS based filter.

2. When $p \neq 0$

As can be seen from Fig. 3, the parameter d controls the fine variations in the cutoff frequency of the filter and the parameter M increases the cutoff frequency range. The new parameter p introduced in the CVFD element increases the range as well as the resolution of the cutoff frequency variation. The various lowpass filter responses that can be obtained from the ICVFD filter when p is also varied are shown in Fig. 4. The cutoff frequency of the modal filter is $f_{c_mod} = 0.2$ and the values of the interpolation factor used for this example are $M = \{1, 2\}$, and the values of the fractional delay parameter are $d = \{0, 0.1, 0.3, 0.7\}$. Only 4 values are used for the parameter d and the zoomed and cropped versions of the responses are shown so as to maintain the clarity of the figure. The values of the parameter p are 0, 1 and 2. The magnitude responses with line style

- 1) 'dash' (the responses in the blue color) are obtained for $p = 0$ and $M = 1$,
- 2) 'solid' (the responses in the red color) are obtained for $p = 0$ and $M = 2$,
- 3) 'dash and dot' (the responses in the black color) are obtained for $p > 0$.

The magnitude responses in the blue color are same as in the case of the FDS based filter. The magnitude responses in blue and red together are same as the lowpass filter responses obtained in Fig. 3 for $M = 1, 2$. As can be seen from the magnitude responses in black color in Fig. 4, when $p > 0$, the range as well as the resolution of the cutoff frequency variations is increased for the same sets of values of the parameters d and M . For instance, let $d = 0.1$. For $p = 0$ and $M = 1$, $D_c = 1.1$. For $p = 0$ and $M = 2$, $D_c = 2.2$. When

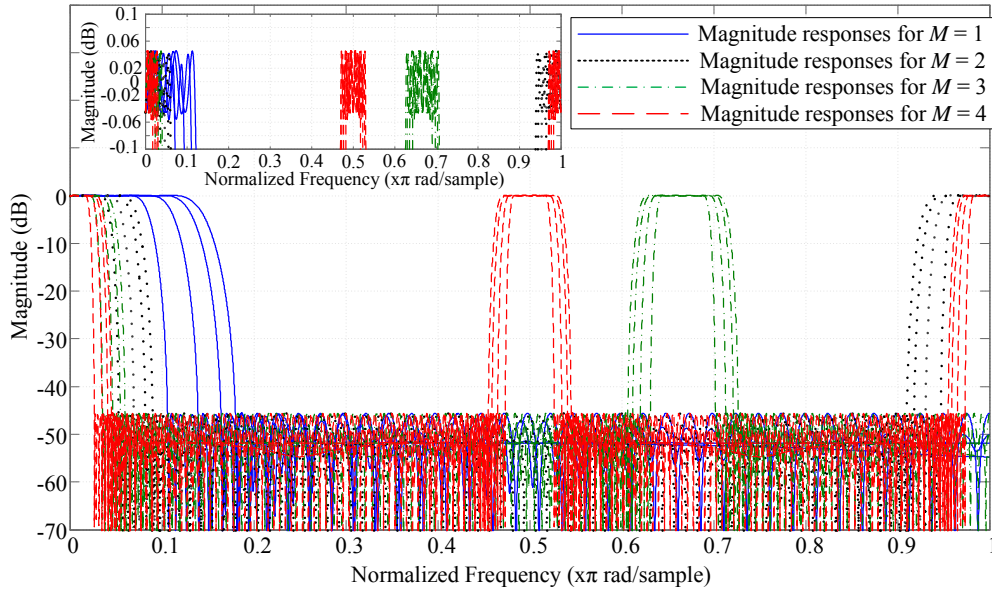


Fig. 3. Multiband responses obtained from the ICVFD filter.

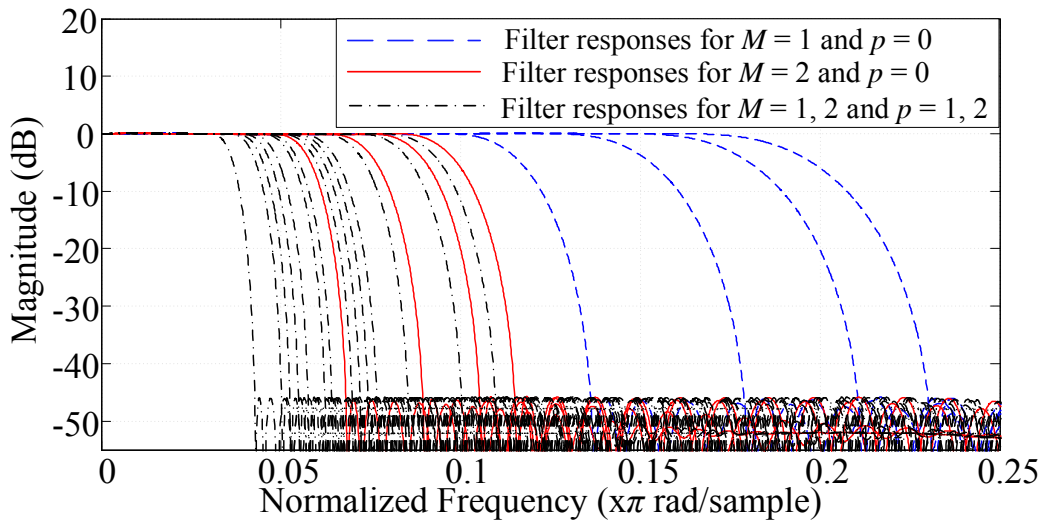


Fig. 4. Lowpass filter responses obtained from the ICVFD filter.

$p = 1$, $D_c = 2.1$ and 3.2 for $M = 1$ and 2 respectively. When $p = 2$, $D_c = 3.1$ and 4.2 for $M = 1$ and 2 respectively. Note that the fractional delay values of 2.1 , 3.2 , 3.1 , and 4.2 , and hence the corresponding cutoff frequencies are not possible in the case of the FDS based filter. The cutoff frequencies corresponding to these fractional delays can be obtained in the ICVFD filter without any increase in the multiplication complexity of the prototype filter structure compared to the FDS based filter. (As the multiplication complexity of the CVFD element is the same as that of the second-order modified Farrow structure, for the same filter order, the total number of multiplications required for the fractional delays remains the same for the ICVFD filter and the FDS based filter.)

D. Properties of ICVFD Filter

1. Passband ripple and stopband attenuation

In the ICVFD filter, all the filter coefficients of the modal filter are used for the filtering operation. Hence, unlike the CDM [6], no degradation occurs in the passband ripple or the stopband attenuation of the resultant ICVFD filter response compared to the prototype filter response. To illustrate this point, the magnitude responses of the prototype

filter and the ICVFD filters (for two different parameter settings) are shown in Fig. 5. The zoomed and cropped versions of the responses are also shown in the inset.

2. Transition bandwidth

As seen from (4), the transition bandwidth of the ICVFD filter is always less than or equal to the transition bandwidth of the prototype filter.

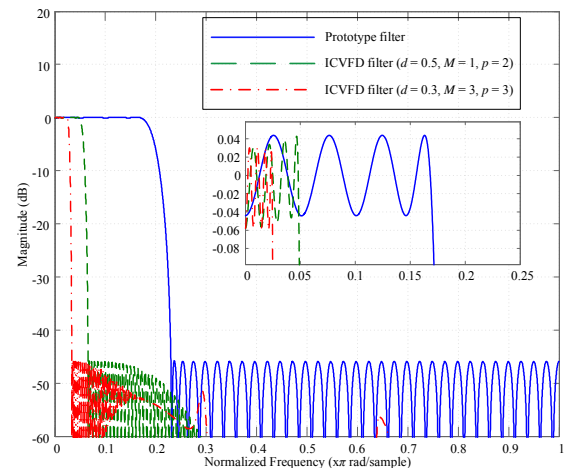


Fig. 5. Magnitude response of the prototype filter and the ICVFD filters.

3. Linear phase

Unlike the all-pass transformation based filter in [7], the ICVFD filter maintains the linear-phase property in its passband region. The magnitude-phase response plots of the ICVFD filter for two different parameter settings are shown in Fig. 6. Phase delay plots are shown in the inset of figures.

4. Cutoff frequency range

By proper choice of the fractional delay value and the interpolation factor, the cutoff frequency of the ICVFD filter can be varied anywhere below the cutoff frequency of the prototype filter (i.e. $f_{c_ICVFD} \leq f_{c_mod}$). One limitation of the proposed ICVFD filter is that $f_{c_ICVFD} \leq f_{c_mod} \leq 0.2$. This is because of the inherent limitation of the fractional delay structure that it provides unity magnitude response and constant phase delay only up to the normalized frequency of approximately 0.2 [13-15]. Beyond this range, the magnitude and the phase delay start deviating from the desired values.

E. Comparisons

The FDS based filter (for $d \geq 0.85$) as well as the ICVFD filter require a low complexity masking filter for suppressing the undesired bands in the filter response. The comparison of the ICVFD filter and the FDS based filter (without and

with CDM) is presented in Table I, for generating the lowpass filter responses. The SPA technique [9] and the technique in [11] are also considered for the comparison. Transposed direct form filter implementation is considered in each case. The desired final specifications are peak to peak passband ripple = 0.1 dB, stopband attenuation = -45 dB, and transition bandwidth = 0.1. All the filters considered for this comparison are designed to satisfy these specifications.

The ICVFD filter is designed with $M = \{1, 2\}$ and $p = \{0, 1, 2, 3\}$. The order of the modal filter is 46, and therefore, when implemented in transposed direct form, it requires 24 multipliers, 46 CVFD elements and 46 adders. Each of the CVFD elements requires 2 multipliers (for multiplication with d) and 5 adders, along with two 2:1 multiplexers for M and one 4:1 multiplexer for p . The order of the masking filter is 38, and it requires 20 multipliers and 38 adders. Therefore, the ICVFD filter requires total 136 (as $24 + 46 \times 2 + 20$) multipliers, total 314 (as $46 + 46 \times 5 + 38$) adders, 92 number of 2:1 multiplexers and 46 number of 4:1 multiplexers.

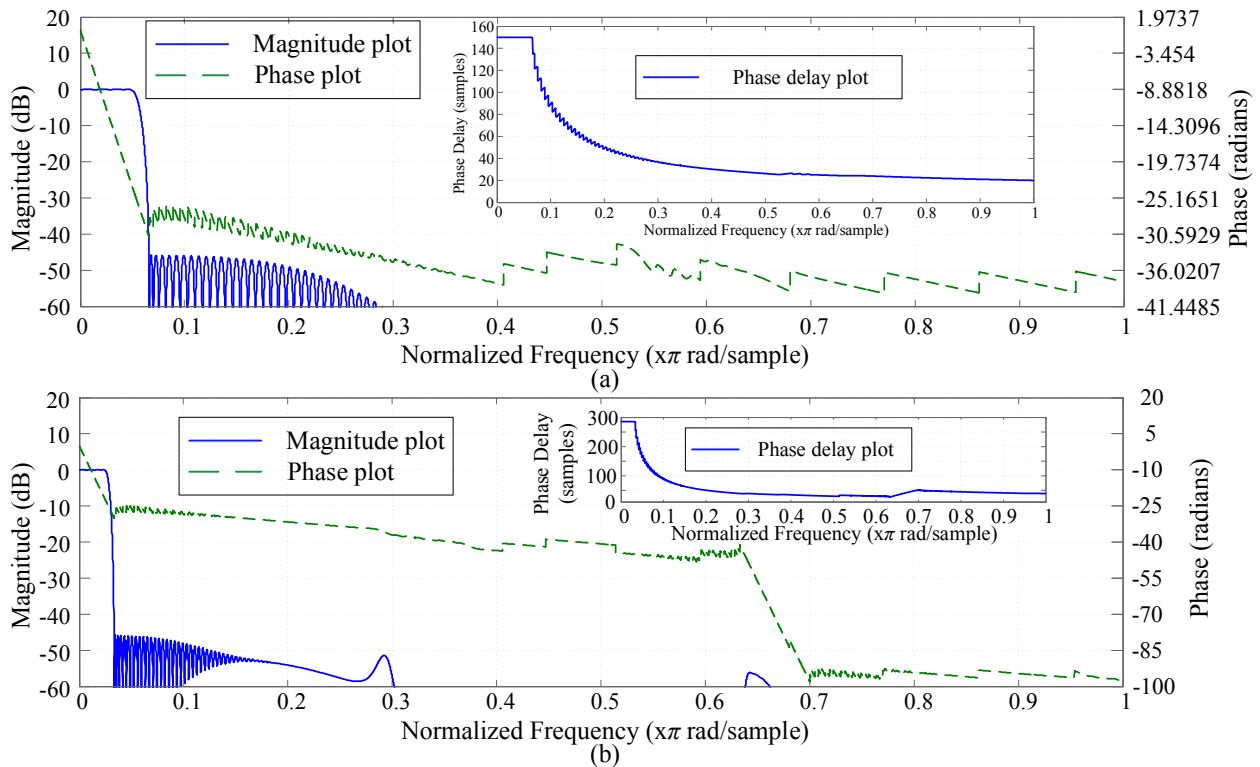


Fig. 6. Magnitude and phase response plots of ICVFD filter (a) for $d = 0.5, M = 1, p = 2$, (b) for $d = 0.3, M = 3, p = 3$.

TABLE I
COMPARISON OF RECONFIGURABLE DIGITAL FILTERS

	Number of				Total gate-count	Cutoff frequency range	Transition bandwidth
	Multipliers	Adders	2:1 mux	4:1 mux			
Proposed ICVFD filter	136	314	92	46	185008	0.0287 to 0.2	0.0143 to 0.1
FDS based filter [12]	122	286	0	0	160436 (-13%)	0.1 to 0.2	0.05 to 0.1
FDS based filter with CDM [12]	282	670	55	0	373548 (+102%)	0.05 to 0.2	0.025 to 0.1
SPA based filter [9]	>250	>500	0	0	>320500 (+73%)	0.0287 to 0.2	0.1
Filter in [11]	>250	>500	0	0	>320500 (+73%)	0.0287 to 0.2	0.1

Similarly, the total number of multipliers, adders, and multiplexers required for each of the filters considered for comparison are presented in Table I. Note that when FDS based filter is combined with the CDM technique, a higher order modal filter, and therefore, more resources are required in order to satisfy the final transition bandwidth and stopband attenuation specifications.

A 16x16 bit multiplier, a 16 bit adder, a 4:1 mux, a 2:1 mux, and a 2-input NAND gate are synthesized on a TSMC 65nm process using the Synopsis Design Compiler. The area of each component is normalized by the area of NAND gate. The total gate-count calculated from these normalized values represents the area of the filter in terms of the equivalent number of NAND gates. The number of multipliers, adders, multiplexers and the total gate-count calculated as explained above is presented in Table I for each of the filters. The ($\pm x$) values in Table I indicate the percentage increase or decrease in the total gate-count for the respective filters when compared with the ICVFD filter. As can be observed, when compared to the FDS based filter, the ICVFD filter offers wider cutoff frequency range and narrower transition bandwidth at the cost of only moderate increase in the area. Alternatively, the FDS based filter with CDM requires 102% more area when compared to the ICVFD filter, for comparable cutoff frequency range and transition bandwidth.

III. HARDWARE REALIZATION OF ICVFD FILTER

In order to realize the ICVFD filter on FPGA, we optimize the filter design in two steps, viz. use of pipelining (for improving operating speed and reducing the resource utilization) and utilization of FPGA specific feature (to improve the operating frequency further).

A. Pipelining for Hardware Implementation

The structure CVFD element is shown in Fig. 1, along with its critical path (shown as 'dash and dot' line with blue color). As can be seen, the critical path of the CVFD element extends from its input to the output. Therefore, as shown in Fig. 2 with 'dash and dot' line with blue color, the critical path of the modal filter of the ICVFD filter consists of a fixed-coefficient multiplier h_0 , N number of CVFD elements and N adders, where N is the order of the modal filter. As the ICVFD filter consists of the interpolated modal filter and a fixed-coefficient masking filter (used to extract the desired band from the multiband response), its critical path extends from its input of the modal filter to the output of the masking filter.

Such a long critical path makes the hardware implementation of the filter design infeasible without any pipelining. To improve the operating frequency, we add two levels of pipelining stages. First, in order to break the long critical path from input to output, a unit delay has been added between the interpolated modal filter structure and the masking filter.

After this first level of pipelining, the critical path is found to be from the input to the output of the interpolated modal filter. Therefore, to break this critical path, one pipelining delay can be added after each of the CVFD elements (second-level pipelining with one unit delay).

In order to shorten the critical path further, instead of

adding one unit delay after every CVFD element, two pipelining delays are added inside each of the second-order modified Farrow structure (second-level pipelining with two unit delays). As the variable multipliers, i.e. the multipliers with one input as d , are the most computationally intensive blocks, these two pipelining delays are inserted in order to separate these blocks. Additional delay elements wherever required are added in the filter structure, such that the overall filter functionality remains unaffected.

B. Hardware Realization of Variable-Length Delays

There are two variable-length delay structures in the ICVFD filter, viz. M variable delays inside the second-order modified Farrow structure (due to the interpolation) and p variable delays (as required in (1)). A straightforward way to implement such variable delays is to use multiple unit delay elements and select the appropriate number of delays using a multiplexer, with a select line with appropriate input for M or p . However, for FPGAs, multiplexers are costly in terms of both resource utilization as well as propagation delay.

As the hardware implementation of the delay element in the filter structure is done by a register, selection of variable number of delay elements (for M as well as for p) can be realized by using the addressable shift registers. We make use of Xilinx's IP core of RAM-based Shift Registers (SRLs) [16] to implement variable-length delays. The IP provides variable-length shift registers, which can be used as variable-length delay elements, with reduction in the propagation delay as well as resource requirement.

IV. IMPLEMENTATION RESULTS

The filter models were created considering the specifications mentioned in Section II-E. These filter models were created using MATLAB Simulink and Xilinx System Generator. The filters are implemented in the Xilinx Virtex 6 xc6vlx760-1ff1760 FPGA, using Xilinx ISE 14.6.

A. Effect of Pipelining

Filter implementation without any pipelining and after the first level of pipelining (i.e. separating the modal filter and masking filter) results in a very long critical path, resulting in infeasible designs. The estimated clock period after synthesis for ICVFD filter design with no pipelining and after first level of pipelining is more than 1000 ns. If one pipelining delay is added after every CVFD element (second-level pipelining with one unit delay), the ICVFD filter implementation becomes feasible with the post-place-and-route (post-PAR) maximum operating frequency of 30 MHz. Use of two pipelining delays inside each of the second-order modified Farrow structures (second-level pipelining with two unit delays) significantly improves the post-PAR maximum operating frequency to 58 MHz.

The implementation results for the interpolated modal filter structure with second-level pipelining with one unit delay and the interpolated modal filter structure with second-level pipelining with two unit delays are presented in Table II. Filter with second-level pipelining with two unit delays requires 84% more slice registers compared to the filter with second-level pipelining with one unit delay. However, due to the compact packing of the logic, it results in reducing the

requirement of LUTs and slices, and improving the post-PAR maximum operating frequency. As the overall area requirement is determined by the number of slices, use of two unit delays for pipelining actually results in reducing the area requirement by 19% and improving the maximum operating frequency by 91%.

B. Effect of SRLs

Pipelining improves the maximum operating frequency as well as reduces the number of occupied slices. To improve the operating frequency and reduce this area requirement further, variable-length delay structure can be realized using SRL instead of multiple delays and a multiplexer. Two ICVFD filter (interpolated modal filter + masking filter) models are created in MATLAB Simulink using the Xilinx System Generator block. One model utilizes multiple unit delay elements and multiplexer and the other utilizes addressable shift registers, which can then be realized as SRLs while generating Verilog implementation. The results are summarized in Table III. Use of SRLs results in reducing the requirement of slice registers by 39%. This results in compact packing of logic and better routing which improves the post-PAR maximum operating frequency by 7%. Use of SRLs also results in small (2%) improvement in overall area requirement (number of occupied slices).

C. Comparison with FDS based Filter

Similar to the pipelining of the ICVFD filter mentioned above, FDS based filter model with second-level pipelining with two unit delays was created. The FPGA implementation results of this FDS based filter are summarized in Table IV,

along with that of the ICVFD filter (for delay elements and multiplexer based design). The specifications are same as that considered for the comparison in Section II-E. The FDS based filter with CDM and filters based on the techniques in [9] and [11] are not considered for this comparison due to their high complexity. As can be observed from Table IV, the FPGA implementation results (increase in number of occupied slices) are in agreement with the theoretically estimated (increase in gate-count) results. The post-PAR minimum period of the ICVFD filter is slightly more than that of the FDS based filter, due to the more complex structure of the CVFD element used in the ICVFD filter when compared to the fractional delay structure used in the FDS based filter.

V. CONCLUSIONS

In this paper a continuously variable fractional delay (CVFD) element is proposed, which is used to replace the unit delay in the prototype filter of the proposed interpolated continuously variable fractional delay structure based filter (ICVFD filter). The CVFD element provides wide fractional delay range at the minimum complexity possible, and is capable of changing the fractional delay range on-the-fly. When compared to the existing fractional delay structure (FDS) based filter, the proposed ICVFD filter has dynamically variable, wider cutoff frequency range. It is also capable of providing variable bandpass and highpass filter responses. The ICVFD filter is suitable for obtaining the variable narrowband responses, especially in the lower

TABLE II
FPGA IMPLEMENTATION RESULTS OF INTERPOLATED MODAL FILTER OF THE ICVFD FILTER FOR DIFFERENT PIPELINING DELAYS

	Number of			Post-PAR minimum period (in ns)	Post-PAR maximum operating speed (in MHz)
	Slice registers	LUTs	Occupied slices		
Interpolated modal filter with second-level pipelining with one unit delay	9559	68800	20104	32.816	30.473
Interpolated modal filter with second-level pipelining with two unit delays	17580 (+84%)	56891 (-17%)	16231 (-19%)	17.203 (-48%)	58.192 (+91%)

TABLE III
FPGA IMPLEMENTATION RESULTS OF ICVFD FILTER FOR DELAY ELEMENTS AND MULTIPLEXER BASED DESIGN AND SRL BASED DESIGN

	Number of			Post-PAR minimum period (in ns)	Post-PAR maximum operating speed (in MHz)
	slice registers	LUTs	Occupied slices		
ICVFD filter with second-level pipelining with two unit delays – delay elements and mux based design	18545	60973	17395	16.69	59.916
ICVFD filter with second-level pipelining with two unit delays – SRL based design	11292 (-39%)	61342 (+1%)	17108 (-2%)	15.635 (-7%)	63.959 (+7%)

TABLE IV
FPGA IMPLEMENTATION RESULTS FOR ICVFD FILTER AND FDS BASED FILTER

	Number of			Post-PAR minimum period (in ns)	Post-PAR maximum operating speed (in MHz)
	Slice registers	LUTs	Occupied slices		
ICVFD filter	18545	60973	17395	16.69	59.916
FDS based filter [12]	12627 (-32%)	54795 (-10%)	15598 (-10%)	15.784 (-5%)	63.355 (+6%)

region of the frequency spectrum. Two-stage approach for the FPGA implementation of the ICVFD filter was presented. It was shown that the FPGA implementation results of are in agreement with the theoretical comparison of the ICVFD filter and the FDS based filter.

REFERENCES

- [1] Woo Jin Oh and Yong Hoon Lee, "Implementation of programmable multiplierless FIR filter with powers-of-two coefficients," *IEEE Transactions on Circuits and Systems II*, vol. 42, no. 8, pp. 553-556, Aug. 1995.
- [2] H. R. Lee, C. W. Jen and C. M. Liu, "A new hardware efficient architecture for programmable FIR filters," *IEEE Transactions on Circuits and Systems II*, vol. 43, no. 9, pp. 637-644, Sept. 1996.
- [3] T. Solla and O. Vainio, "Comparison of programmable FIR filter architectures for low power," *Proceedings of 28th European Solid-State Circuits Conference*, pp. 759-762, Italy, Sept. 2002.
- [4] K. H. Chen and T. D. Chiueh, "A low power digit-based reconfigurable FIR filter," *IEEE Transactions on Circuits and Systems II*, vol. 53, no. 8, pp. 617-621, Aug. 2006.
- [5] R. Mahesh and A. P. Vinod, "Reconfigurable frequency response masking filters for software radio channelization," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, issue 3, pp. 274-278, March 2008.
- [6] R. Mahesh and A. P. Vinod, "Low complexity flexible filter banks uniform and non-uniform channelization in software radios using coefficient decimation," *IET Circuits, Devices and Systems*, vol. 5, no. 3, pp. 232-242, May 2011.
- [7] A. G. Constantinides, "Spectral transformations for digital filters," in *Proceedings of the Institution of Electrical Engineers*, vol. 117, no. 8, pp. 1585-1590, Aug. 1970.
- [8] S. C. D. Roy and S. S. Ahuja, "Frequency transformations for linear-phase variable cutoff digital filters," *IEEE Transactions on Circuits and Systems*, vol. 26, no. 1, pp. 73-75, Jan. 1979.
- [9] S. C. Chan, C. K. S. Pun and K. L. Ho, "A new method for designing FIR filters with variable characteristics," *IEEE Signal Processing Letters*, vol. 11, no. 2, pp. 274-277, Feb. 2004.
- [10] P. Lowenberg and H. Johansson, "Minimax design of adjustable-bandwidth linear phase FIR filters," *IEEE Transactions on Circuits and Systems I*, vol. 53, issue 2, pp. 431-439, Feb. 2006.
- [11] H. Johansson and P. Lowenberg, "On linear phase FIR filters with variable bandwidth," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 51, no. 4, pp. 181-184, Apr. 2004.
- [12] S. J. Darak, A. P. Vinod and E. M-K. Lai, "A new variable digital filter design based on fractional delays," *IEEE International Conference on Acoustics, Speech and Signal Processing*, pp. 1629-1632, Prague, Czech Republic, May 2011.
- [13] V. Valimaki, "A new filter implementation strategy for Lagrange interpolation," *IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 361-364, USA, May 1995.
- [14] T. I. Laakso, V. Valimaki, M. Karjalainen, and U. K. Laine, "Splitting the unit delay," *IEEE Signal Processing Magazine*, vol. 13, no. 1, pp. 30-60, Jan. 1996.
- [15] C. Candan, "An efficient filtering structure for Lagrange interpolation," *IEEE Signal Processing Letters*, vol. 14, no. 1, pp. 17-19, Jan. 2007.
- [16] DS222: LogiCORE IP RAM-based Shift Register, Xilinx, 2011.