

Applications, Prospects and Challenges of Silicon Carbide Junction Field Effect Transistor (SiC JFET)

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¹Abstract—properties of Silicon Carbide Junction Field Effect Transistor (SiC JFET) such as high switching speed, low forward voltage drop and high temperature operation have attracted the interest of power electronic researchers and technologists, who for many years developed devices based on Silicon (Si). A number of power system Engineers have made efforts to develop more robust equipment including circuits or modules with higher power density. However, it was realized that several available power semiconductor devices were approaching theoretical limits offered by Si material with respect to capability to block high voltage, provide low on-state voltage drop and switch at high frequencies. This paper presents an overview of the current applications of SiC JFET in circuits such as inverters, rectifiers and amplifiers. Other areas of application reviewed include; usage of the SiC JFET in pulse signal circuits and boost converters. Efforts directed toward mitigating the observed increase in electromagnetic interference were also discussed. It also presented some areas for further research, such as having more applications of SiC JFET in harsh, high temperature environment. More work is needed with regards to SiC JFET drivers so as to ensure stable and reliable operation, and reduction in the prices of SiC JFETs through mass production by industries.

Keywords— Amplifier, Boost Converter, Electromagnetic Interference, Inverter, JFET, Rectifier, SiC JFET, Silicon Carbide.

I. INTRODUCTION

Initial efforts to develop silicon carbide Junction Field Effect Transistor (SiC JFET) was in the early 1990s. However, the device' relatively low transconductance, low channel mobility and challenging fabrication process were its major drawback. Subsequently, by mid-2000s, after further research and improvement, the first prototype SiC JFET was produced [1]. SiC JFET has attractive properties such as high switching speed, low forward voltage drop and high

temperature operation, which have drawn the attention of power electronics research community, who for decades developed devices based on silicon (Si). More so, many power system Engineers have been searching for alternative solutions to silicon devices in order to develop more robust equipment that requires higher power density circuits and modules. It was observed that several available power electronic devices offered by semiconductor materials were approaching their ideal performance limits with respect to capability to block high voltage, provision of low on-state voltage drop and high switching frequencies. The most promising approach was to replace Si in the fabrication of power semiconductor devices with a wider bandgap material with acceptable bulk mobility, such as SiC and gallium nitride (GaN). In this context, SiC offers great potential for the realization of high power devices owing to its attractive properties. When compared with Si materials they have ten times higher breakdown electric field; three times wider band gap - about 3 eV at 27 °C and higher thermal conductivity; and two times higher saturation velocity [2], [3]. In addition, intrinsic charge carrier concentration of SiC material is lower than the corresponding value for Si which is principally attributed to the wide band-gap of SiC [4]- [9]. Among the several polymorph of SiC, 4H- and 6H-SiC have gained the attention of researchers [4], [9], however, 4H-SiC is the most commonly used in the fabrication of SiC JFET due its preferred channel charge mobility [10].

Meanwhile, modeling of the JFET has received significant attention by researchers [2], and most of these models are derivatives of the Shockley's equation, shown in (1) [11]; I_{DS} is the drain current, I_{DSS} is drain current at saturation when pinch-off voltage, V_P is attained. The gate-to-source voltage V_{GS} , is the controlling quantity, while I_{DS} is the controlled quantity:

$$I_{DS} = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2. \quad (1)$$

Device property is parameterized by thickness, length, width and doping concentration of channel and charge mobility. And there is a need to extensively evaluate JFETs physical models, in terms of their behaviour with temperature, transfer and output characteristics, and changes in channel length [10]. The V-I characteristics of SiC JFET can effectively be modeled by the same model developed for long-channel silicon devices. This is true, although, SiC has wider band gap than Si and possesses multiple-donor levels, thus making the relationship between the impurity

Manuscript received April 29, 2016 revised June 30, 2016 revised September 10, 2016.

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concentration and the carrier density complex [12]. From [12], the drain current of SiC JFET is given by (2) as:

$$I_{DS} = \left(\frac{W}{L}\right) I_p' (1 + \lambda V_{DS}) \left[\frac{3V_{DS}}{V_p} - 2 \left\{ \frac{(V_{DS} - V_{GS} + V_{bi})}{V_p} \right\}^{3/2} - \left\{ \frac{(-V_{GS} + V_{bi})}{V_p} \right\}^{3/2} \right], \quad (2)$$

where:

W = width of channel

L = length of channel

V_{bi} = built-in voltage of the gate-channel junction

V_p = pinch-off voltage

I_p' = normalized pinch-off current

λ = channel length modulation parameter

Built-in voltage of the gate-channel junction V_{bi} is a function of the temperature T , doping densities in the P^+ -gate N_A and n-channel N_D , and intrinsic carrier density n_i . The relationship is as shown in (3):

$$V_{bi} = \frac{KT}{q} \ln \left(\frac{N_A N_D}{n_i^2} \right), \quad (3)$$

where K and q are Boltzmann and electron charge constants respectively. Whereas, the pinch-off voltage, given in (4) depends on the depth of channel D and permittivity of the channel ϵ_s .

$$V_p = \frac{qN_D D^2}{2\epsilon_s}. \quad (4)$$

Normalized pinch-off current is represented by (5) as:

$$I_p' = \frac{q^2 N_D n \mu_n D^3}{6\epsilon_s}, \quad (5)$$

where n and μ_n are the ionized carrier density in the channel and carrier mobility.

Fig. 1 shows the cross section of SiC JFET. The types and structures of the JFET is thoroughly discussed in [1], [13], and from which Fig. 2 showing a SiC JFET family tree was drawn. Operating principle of the power JFET is modulation of the channel depletion region through the applied gate-to-source voltage. If the gate-to-source voltage, V_{GS} is higher than the gate threshold voltage, the JFET begins to conduct and a current can be established in the channel. The gate threshold voltage is the boundary

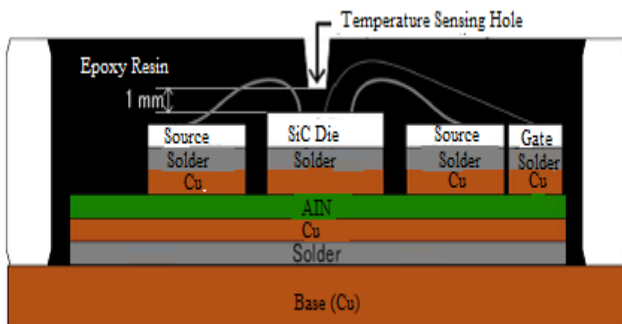


Fig. 1: A cross sectional view of SiC JFET, which was jointly developed by KEK and Sun-A corporation. The device is assembled on a 58 mm x 36 mm copper based plate and have the height of 7 mm. The size of the die is 4.16 mm x 4.16 mm, which was manufactured by SiCED (Germany) [67]

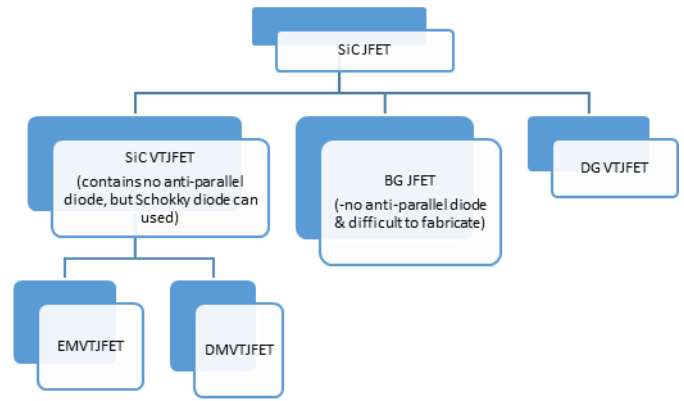


Fig. 2: SiC JFET family tree, available structures are Silicon Carbide Lateral Channel Junction Field Effect Transistor (SiC LCJFET), Silicon Carbide Vertical Trench Junction Field Effect Transistor (SiC VTJFET) - comprising of Enhancement-Mode Vertical Trench Junction Field Effect Transistor (EMVTJFET) and Depletion Mode Vertical Trench Junction Field Effect Transistor (DMVTJFET); Buried Grid Junction Field Effect Transistor (BG JFET), and Double Gate Vertical Trench Junction Field Effect Transistor (DG VTJFET)

between the conduction and the blocking area [13] with the drain current depending on the amount of the voltage barrier occurring in the channel [14].

In this paper an overview of published SiC JFET based circuit applications and evaluations is presented in Section II. While Section III highlights current challenges and suggested areas for future research with respect to SiC devices. Finally, conclusions reached are reported in Section IV.

II. OVERVIEW OF SiC APPLICATION

A. SiC JFET Application in Rectifiers and Amplifiers Circuits

Hybrid rectifiers made from Junction Barrier Schottky (JBS) rectifier and Trench JFET Schottky rectifier (TJFET), which combines the merits of Schottky rectifiers otherwise known as hot carrier diode with the advantages of PiN diode rectifiers was presented in [15]. The merits of Schottky rectifiers are better on-state and switching performance owing to the unipolar nature of Schottky diode, hence, no charges are stored and no depletion layer is formed. On the other hand, merits of PiN diode rectifiers are superior reverse leakage and breakdown characteristics, which are due to its intrinsic semiconductor layer leading to a decrease in the capacitance of the P-N region.

Furthermore, [15] measured and optimize the conductivity modulation in the hybrid rectifier. Analysis and characterization of the dynamic behaviour of a cascade rectifier base on normally-ON (N-ON) SiC JFET were carried out in [16]. Here the authors compared Si MOSFET and SiC JFET based rectifiers with Si rectifier and front-end rectifier, using boost converter incorporating power factor corrector (PFC)-used for generating ac output signals connectable to one or more loads, such as capacitive loads. It concluded that the SiC JFET based rectifier behaved poorer than the Si ultrafast diode rectifiers, in terms of reverse recovering time and current. But the recovering time of SiC JFET is lower than that of Si MOSFET, thus making SiC JFET more suitable for high speed rectification and bidirectional switch applications. Similar conclusions were reached by authors in [17], who characterized the reverse

conduction characteristics of normally-off SiC JFET using diode techniques.

A 30V supply precision operational amplifier (op-amp) designed to support industrial, instrumentation, and other application was realized using Auto-zeroing and chopping in [18] employing JFETs and Bipolar Junction Transistors (BJTs), with performance less than that of complementary metal oxide semiconductor field effect transistor (CMOS). CMOS based precision amplifier was superior because of cheaper wafer prices, reduced offset voltage, and so on. A transimpedance amplifier (TIA) based low-noise, wideband amplifier used in detecting 1064nm laser generated noise in quantum optical experiment was reported in [19]. The TIA, which conceptually, is a current-to-voltage converter and most frequently implemented using operational amplifier, performed better than single-junction field effect transistor based amplifier. Additionally, the design, development and characterization of a high gain RF amplifier for very low frequency receiver application using JFET and op-amp was presented in [20]. At 19.8 kHz, the design criteria was satisfied with a satisfactory gain of 46.003dB. Moreover, evaluation of the capability of a SiC JFETs for an induction synchrotron has been carried out. The device was operated with a repetition rate of 1 MHz, a drain-source voltage of 1 kV, and a drain current of 50 A in burst mode [21]. A synchrotron is a cyclic particle accelerator capable of generating extremely powerful x-rays. A presentation of experimental and simulation results involving an ac solid state variable current limiter circuit using 1200V SiC JFETs as an additional current limiting circuit for high power amplifiers to test power factor correction circuit was given in [22].

B. SiC JFET Application in Pulse Signal circuit

It was noted in [23] that SiC depletion mode JFET are well suited for pulse power applications as an opening switch due to their normally-ON nature. Also, the maximum avalanche energy of the device under repetitive condition was determined. The approach employed involves driving the N-ON SiC JFET has a nominal rating of 1200V/13A into punchthrough breakdown by using UIS circuit. Whereas development and description of a two-channel time-delay pulse signal generator was presented in [24]. According to [25], SiC JFET has been evaluated on an optimized double pulse circuit, where it shows switching energies four times lower than its equivalent Silicon Insulated Gate Bipolar Transistor (Si IGBT). Moreover, the performance characteristics along with the switching behaviour of a large area 6500V normally off JFETs and JBS diodes using double pulse testing at 3000V/11A with an inductive load was reported in [26], which is higher than the single 3300V application reported in [27]. However, the use of JBS diode was eliminated in [28], where a normally-off (N-OFF) SiC JFET was operated in cascode with a Si IGBT to unify the gate driver voltage and increase the switching speed of the JFET. This configuration was necessitated by the incompatibility of gate drive voltage of JFET and IGBT based FREEDM-pair, which increases the complexity and cost of the circuit. A balancing circuit that results in faster switching transients and higher operating pulse current was presented in [29]. It also reported an R-C network, which enhances the dynamic behaviour of the supercascode of SiC JFET/Si MOSFET. More so, SiC JFET/Si MOSFET cascade

control methods was reported in [30].

C. SiC JFET in and Electromagnetic Interference Consideration

In [31], it was noticed that SiC based devices leads to an increased electromagnetic interference (EMI) production level. In addition, according to [31] SiC based circuits can record switching loss decrease of up to 70% in a comparison with the switching losses of Si, Si-SiC and SiC device combinations. It can pave way for the application of SiC JFET in low-voltage industrial variable-speed drives of 1200 V SiC-based devices, currently dominated by Si IGBTs and diodes. The authors in [32] reported the development of the popular 1200V/30A SiC JFET module using a half bridge topology. It consist of three-single SiC JFET chips connected in series with two parallel low voltage P-MOSFETs. This configuration help to overcome the normally-on problem of JFETs, which leads to loss of control and undesired conduction of switches. Furthermore, this may lead to shoot through current damaging the power system. This topology also makes them suitable in efficiency sensitive sections of renewable energy and uninterrupted power supply systems.

However, a non-contact signal transfer mechanism for transferring multiple signals over a rotational interface through electromagnetic means was described in [33]. The mechanism is built for space crafts. The work reported in [34], dealt with electromagnetic interference in a SiC JFET inverter. It proposed integrating small-value common-mode (CM) capacitors into the inverter so as to minimize EMI. A reduction in the CM conducted emissions was noticed, though, this approach resulted in slight increase in the system losses, system size, and poorer switching waveforms. Meanwhile, [35] proposed a method of characterizing interelectrode capacitances, which will allow for effective study of SiC JFET switching waveform during interelectrode capacitance evolution. The operating range of the JFET was optimized so as to achieve uniform gain during amplitude modulation. Its benefits and limitations were discussed for space craft application. On the other hand, dv/dt control methods for a SiC JFET/Si MOSFET cascade aimed at avoiding the impairment to electromagnetic compatibility, which could result from the transient for hard commutation reaching values up to 45 KV/ μ s, when there is no control was reported in [30].

D. SiC JFET Application in Inverter and Boost Converter Circuit

A 10kW three phase (3 - ϕ) bidirectional on-board battery charger for use as a vehicle to grid (V2G) interface in electric vehicles was reported in [36]. It incorporated a 1200V SiC JFET, which enables the device operation at high voltage in the dc link and high switching frequency ranging between 50-150 kHz, while an IGBT boost converter serves as interface to the grid. Moreover, an evaluation of a high frequency boost converter module was reported in [37]. Whereas, in [38], a step-up oscillator configuration using a piezoelectric transformer and a JFET capable of enabling a boost dc/dc converter the moment the start-up circuit outputs enough voltage. The design of a 40kVA inverter, with an efficiency, greater than 99.5% using Si JFET was presented in [39]. The implementation involved ten 85 m Ω N-ON JFET in parallel, in each switch position, this will reduce

conduction losses. The inverter performs better than Si IGBT based inverter.

An experimental demonstration of the use of vertical SiC JFET in an inverter leg without external free-wheeling diodes was shown in [13]. This was achieved by taking advantage of the reverse conduction capability of the device. A presentation of a 3 KVA 1220v/6A with switching speed of 200 KHz all-SiC JFET current source converter, with reduced size and weight in comparison with its Si MOSFET equivalence was reported in [40]. In presenting a dc/dc boost converter, the authors in [6] compared N-ON JFET devices having a threshold voltage of 50v and -10v with BJT devices with a view of extracting the maximum performance of the devices and thereafter, choosing the optimal driving condition. It concluded that the conduction losses of both types of devices is not a function of the switching frequency. Whereas the driver loss of the BJTs seem not to be dependent on the switching frequency, the driver loss of JFET devices is proportional to the switching frequency. This comparison was repeated in a modular multilevel converter, where it was reported that SiC JFET can be used without anti-parallel diode. Hence, the body diode can be used during the switching transients to achieve an efficiency of up to 99.8%, which was achieved in a 300 MW 3.3 kV 1.2 kA SiC JFET converter. However, the choice of no anti-parallel diode is not available in Si MOSFET based devices [9].

The better efficiency of JFET over BJT is partly due to BJT requirement of a continuous base current when collector current flows. This warrants the purchase of a supply transformer for base drive circuit [41], [42]. Moreover, the authors in [9] reported dc/dc converters made of SiC JFET and SiC MOSFET with the former possessing a slightly higher efficiency of 96% as against the 95.5% of the latter, with weak frequency dependency. However, a cascode of Si MOSFET and SiC JFET possesses an efficiency of 98% at frequency range of 400 kHz to 1 MHz. The high efficiency of SiC JFET is enhanced by the absence of the Miller effect since it operates in the common-gate configuration, hence lower switching losses. On the other hand, SiC MOSFET possesses lower efficiency due to higher on-state resistance and parasitic capacitance. It is noted that a dc/dc boost converter steps up voltage while stepping down current from its supply to its load. It is a switch-mode power supply (SMPS) usually containing any of the following switches; MOSFET, IGBT or BJT. Development and testing of high frequency, high efficiency inverter using a SiC JFET power module, shown in Fig. 3 was presented in [8]. Its approach was to employ a rugged negative voltage gate drive to overcome the N-ON issue associated with JFET devices and to avoid the bridge short-through during switching on and off. The developed circuit has a turn-on and turn-off times better than that of Si IGBT based inverter. Its efficiency was higher as well.

Accordingly, the authors in [43] reported application of JFET in converters with operating temperature above 200 °C. Lateral depletion-mode 4H-SiC n-channel JFETs have been reported to have good performance at temperatures ≤ 600 °C, which can prove useful in environments such as fuel combustion chambers in vehicles, deep-well drilling, planetary instrumentations, and other harsh environments [44]. This was verified in [45] through demonstration of ICs based on 4H-SiC JFET integrating Hafnium ohmic contact with TaSi₂ interconnect with SiO₂ and SiN₄ dielectric layer

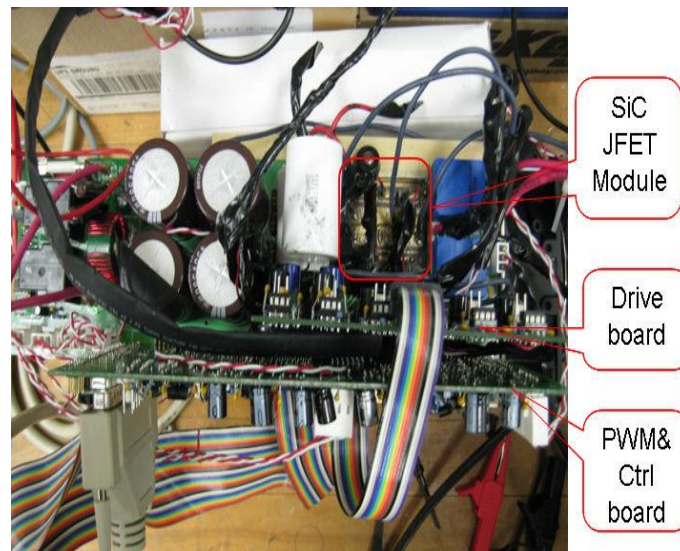


Fig. 3: SiC module based inverter circuits [8]

based on 4H-SiC JFET integrating Hafnium ohmic contact with TaSi₂ interconnect with SiO₂ and SiN₄ dielectric layer over about 1 μ m scale topology designed to withstand 1000 hours of stable electrical operation at 500 °C in the air. The research was extended further by testing the ICs at 727 °C, after 25 hours of operation little change in electrical properties was noticed due to a quick increase in device resistance [46]. However, when the IC die is attached to gold paste, it operated at 700°C for about 144 hours [47]. These results are higher than that of SiC MOSFET devices with operating temperature of about 200°C due to associated oxide interface problems [42]. In addition, SiC CMOS circuits tested to operate at 300 °C under probe and 540 °C when packaged was reported in [48].

E. SiC JFET Application in Short Circuit Detection

A SiC JFET with an incorporated short circuit protection was reported in [49]. Here a short circuit detection is added to a typical driver design. Furthermore, the robustness of 1200V N-ON SiC JFETs against short circuit were examined via experimental parametric analysis and 3-dimensional thermal model simulations in [50]. Merits of this report included presentation of a more accurate and realistic analysis of short circuits outside the power converter where a large stray inductance exists.

F. SiC JFET Application in Circuit Breaker

A new self-powered solid state circuit breaker (SSCB) concept using N-ON SiC JFET as the main static switch was presented in [53], [54]. When testing the suitability of SiC JFET with a N-ON recessed implanted gate vertical-channel feature for light triggered solid state circuit breaker with a 1200 V rating, [55] carried out 2.4 million pulses hard switch at a repetition rate of 10Hz from a blocking voltage of 1200 V to an on-state current of more than 13 times the rated current at 150 °C. A low inductance RLC circuit was used, in which stored energy in the capacitor is discharged in a resistor via SiC JFET. It was observed that the on-state conduction improved slightly, while blocking voltage remain the same. In principle, the SSCB is capable of interrupting current within a short duration, in the order of 10⁻⁶ s without arc formation and no voltage reversal is required. They are usually implemented with gate commutated turn-off thyristors and gate turn-off thyristors. The high on-state

losses of IGBT limits their usage in circuit breakers, although they have the ability of limiting current automatically [56]-[58]. This device uses power sourced from the short circuit faults to turn and hold off the SiC JFET device. Meanwhile, the authors in [59] analyzed a solid state circuit breaker incorporating an isolated dc/dc low power converter with fast-starting property serving as the protection driver. Here, short circuit is detected by sensing a rise in terminal voltage. The SiC JFET based system was able to repeatedly interrupt a fault current of up to 180A at a bus voltage of 400 VDC with an interruption time of 0.8 μ s. The performance of 1200 V SiC N-ON vertical JFET during unclamped inductive switching (UIS) scenario was investigated in [60] by performing UIS tests, a high stress test for characterizing the ruggedness of a device. This was used to observe the energy density. Maximum device temperature during UIS were subsequently forecasted through simulation. This also helped in understanding JFETs failure modes. A presentation of 3500V/15A power module based on SiC JFET and Schottky barrier diodes was given by [61]. The device showed a superior turn-on and turn-off of less than 15ns. It claims to be the first demonstration of SiC JFET power module at a voltage level greater than 3300 V. Meanwhile, a fully integrated six-pack power module consisting of four parallel SiC JFET and two anti-parallel Schottky diode with each module rated 1200 V 100 A, and having the capacity to withstand a temperature up to 200 $^{\circ}$ C with on-state resistance of 55m Ω . However, when implemented in a liquid cooled 3- Φ 5 kW inverter, having an efficiency of 98.5%, the coolant temperature was 95 $^{\circ}$ C. The authors also included a thermal shock test of the module assembly.

G. Miscellaneous Application of SiC JFET

Although SiC JFET is available primarily in 1200V, 1700V also exists with a current rating of up to 48A. The on-state resistance ranges from 45 – 127 m Ω at 27 $^{\circ}$ C, depending on whether it is N-ON- or N-OFF SiC JFET [1], [42], [51]. Moreover, the on-state resistance of 4H-SiC JFET may be up to 400 times lower than that of Si at a specific breakdown voltage. Thereby permitting its use in high current circuits with a comparatively lesser forward voltage drop [3]. The N-OFF SiC JFETs are more recent and desirable than N-ON SiC JFET [17].

An input buffer with monolithic integrated JFET in standard Bipolar-CMOS-DMOS (BCD) technologies process was presented in [52]. It further made a comparison with a buffer having P-channel MOSFET. It was observed that the JFET buffer out performs its P-channel MOSFET counterpart in terms of its low-frequency input referred noise.

An evaluation of the operation of depletion mode SiC JFET was carried out in [24] by developing a dc-dc step-down converter with realistic operating conditions. Then, the functionality of the entire system was verified through measurements. An attempt was made to address the problem of high cost militating against the large scale production and adoption of SiC power devices in [62], through a proposition of a hybrid power module using SiC JFET in parallel with Si IGBT. By so doing, it combined the merits of both transistors. The hybrid power module has a superior cost/performance figures [37], [62].

The effect of parasitic turn-on on a half-bridge with 1700V N-ON SiC JFET-containing 32 pairs of chips in

parallel were tested by [63], while the effect of ion, electron and neutron radiation on the electrical properties and thermal stability of 1700 n-type 4H-SiC epilayer used in fabricating devices such JFETs were examined by [64]. The effect on device properties were analyzed by capacitance deep level transient spectroscopy (DLTS), V-I curve and C-V profiling. It further described how to reduce the effect of parasitic turn-on through a special gate-drive concept, combined with a low inductance design. Moreover, [65] presented three different ways of minimizing parasitic turn-on for a gate-drive unit level circuitry. Of the three proposed solutions, the use of active current sources and clamping can substantially reduce losses. Furthermore, [66] reported a hybrid MOSFET-JFET concept aimed at suppressing Si MOSFET parasitic capacitance effect. Conceptually, parasitic capacitance or stray capacitance exists in sections of electronic circuitry owing to proximity of components to each other. Hence, there is a need to research on device packaging and component placement. Thus, a high power discrete SiC JFET package for accelerator application having a repetition rate of 1 MHz was developed and tested in [67].

III. CURRENT CHALLENGES AND AREAS FOR FUTURE

There are still challenges that should be surmounted so as to unleash the full potentials of not just SiC JFET, but also of SiC MOSFET. This section of the paper highlights some of these and areas for future research. More work is needed so as to better appreciate the trade-off between SiC JFET switching losses and dv/dt – rate in the course of converter design [30]. Hence, further researches are needed in the area of electromagnetic interference mitigation when implementing SiC JFET in a switching circuit. Could the blocking voltage of SiC JFET be extended further? Future studies would provide the answer to this. More applications of SiC JFET in harsh, high temperature environment are expected in the future [1], [44], [68], however, according to [1] there is a need to research on the stability of the device in such environment, develop packages and other accessories that can stand such high temperature environment. For example, in a review of the development of 6H-SiC JFET by NASA for extreme temperature for application analog amplifier, digital logic gates ICs and amplifier circuits [12], reported the use of ceramic packages of Al₂O₃ and gold metallization.

In spite of the work reported in [62], which attempted to address the high cost problem of SiC materials, SiC devices are still more expensive than Si devices. Hence, there is the need to research more in the mass production of SiC JFET. Additionally, more work still needs to be done with regards to SiC JFET drivers so as to ensure stable and reliable operation. In order to fully exploit the potentials of SiC devices, researcher have went as far as developing SiC MOSFET. Some of the examples of SiC MOSFET circuit application are reported in [69]-[73]. The future will see a lot of research in the fabrication of SiC MOSFET, such as studying the reliability and stability of the oxide layer over an extended period of time [1].

IV. CONCLUSION

This review has highlighted the most advance applications of SiC JFET in the literature. Current challenges and areas for further research were discussed. More research is needed so as to facilitate the production of SiC JFET in

commercial quantity, this will bring down the prices in comparison with other switches like BJT and IGBT.

REFERENCES

- [1] R. Jacek, P. Dimosthenis and N. Hans-Peter, "Silicon carbide power transistors: a new era in power electronics is initiated," *IEEE Industrial Electronics Magazine*, vol. 6, no. 2, pp. 17-26, 15 June 2012.
- [2] E. Platania, Z. Chen, F. Chimento, A. E. Grekov, R. Fu, L. Lu, A. Raciti, J. L. Hudgins, H. A. Mantooth, D. C. Sheridan, J. Casady and E. Santi, "A physics-based model for a SiC JFET accounting for electric-field-dependent mobility," *IEEE Transactions on Industry Applications*, vol. 47, no. 1, pp. 199-211, 2011.
- [3] V. Veliadis, "Silicon carbide junction field-effect transistors (SiC JFET)," *Wiley Encyclopedia of Electrical and Electronics Engineering*, pp. 1-37, 2014.
- [4] F. Roccaforte, F. Giannazzo, F. Iucolano, J. Eriksson, M. Weng and V. Raneri, "Surface and interface issues in wideband gap semiconductor electronics," *Applied Surface Science*, vol. 256, no. 19, pp. 5727-5735, 2010.
- [5] H. Choi, "Overview of Silicon Carbide power devices," Fairchild Semiconductor.
- [6] J.-K. Lim, G. Tolstoy, D. Pefitsis, J. Rabkowski, M. Bakowski and H.-P. Nee, "Comparison of total losses of 1.2 kV SiC JFET and BJT in dc-dc converter including gate driver," *Materials Science Forum*, Vols. 679-680, pp. 649-652, March 2011.
- [7] B. Wrzecionko, D. Bortis and J. W. Kolar, "A 120°C ambient temperature forced air-cooled normally-off SiC JFET automotive inverter system," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2345-2358, May, 2014.
- [8] X. Zheng and P. Sanbo, "Design and analyse of silicon carbide JFET based inverter," *WSEAS Transactions on Circuits and Systems*, vol. 11, no. 9, pp. 295-304, 2012.
- [9] R. R. Devarapally, "Survey of applications of WBG devices in power electronics," Kansas, 2016.
- [10] M. Lades, "Modeling and simulation of wide bandgap semiconductor devices: 4H/6H-SiC," 2000.
- [11] O. A. Akpaida, O. Omoroguiwa and M. S. Okundamiya, Principles of electronic devices and circuits, 1st ed., Solozone, Ed., Benin-City, Edo-State: Stemic Publication, 2005.
- [12] P. G. Neudeck, S. L. Garverick, D. J. Spry, L.-Y. Chen, G. M. Beheim, M. J. Krasowski and M. Mehrehany, "Extreme temperature 6H-SiC JFET integrated circuit technology," *Physica status solidi*, 2009.
- [13] R. Ouaida, X. Fonteneau, F. Dubois, D. Bergogne, F. Morel, H. Morel and S. Oge, "SiC Vertical JFET pure diode-less inverter leg," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, Long Beach, CA, 2013.
- [14] S. Bellone, L. Di Benedetto and G. Licciardo, "A model of the off-behaviour of 4H-SiC power JFET," *Solid State Electronics*, vol. 109, pp. 17-24, 2015.
- [15] M. Quddus, M. Mudholkar and A. Salih, "Carrier separation technique to optimize conductivity modulation in high voltage rectifiers," in *Electron Devices and Solid-State Circuits (EDSSC), 2015 IEEE International Conference on*, 2015.
- [16] A. Vazquez, A. Rodriguez, M. Fernandez, M. M. Hernando, E. Maset and J. Sebastian, "On the use of front-end cascode rectifier based on a normally-on SiC JFET and Si MOSFET," *IEEE Transaction on Power Electronics*, vol. 29, no. 5, pp. 2418-2427, May 2014.
- [17] R. Shillington, P. Gaynor, M. Harrison and W. Heffernan, "Silicon carbide JFET reverse conduction characteristics and use in power converters," *IET Power Electronics*, vol. 5, no. 8, pp. 1282-1290, 2012.
- [18] Y. Kusuda, "5.1A 60V auto-zero and chopper operational amplifier with 800kHz interleaved clocks and input bias-current trimming," in *Solid-State Circuits Conference - (ISSCC), 2015 IEEE International*, San Francisco, CA, 2015.
- [19] H. Zhou, W. Wang, C. Chen and Y. Zheng, "A low-noise, large-dynamic-range-enhanced amplifier based on jfet buffering input and JFET bootstrap structure," *Sensors Journal, IEEE*, vol. 15, no. 4, pp. 2101-2105, April 2015.
- [20] R. Putera, Kusnandar, A. Najmurokhman, Sunubroto, Chairunnisa and A. Munir, "High gain RF amplifier for very low frequency receiver application," in *Information Technology and Electrical Engineering (ICITEE), 2014 6th International Conference on*, 2014.
- [21] H. T. Keiichi Ise, K. Takaki, M. Wake, K. Okamura, K. Takayama and W. Jiang, "Development of a megahertz high-voltage switching pulse modulator using a SiC-JFET for an induction synchrotron," *IEEE Transactions on Plasma Science*, vol. 39, no. 2, pp. 730-736, 7 February 2011.
- [22] W. Konrad, K. Leong, K. Krischan and A. Muetze, "A simple SiC JFET based AC variable current limiter," in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, 2014.
- [23] B. Pushpakaran, M. Hinojosa, S. Bayne, V. Veliadis, D. Urciuoli, N. El-Hinnawy, P. Borodulin, S. Gupta and C. Scozzie, "Evaluation of SiC JFET performance during repetitive pulsed switching into an unclamped inductive load," *Plasma Science, Transaction on*, vol. 44, no. 10, pp. 2968-2973, October 2014.
- [24] J. Bacmaga, K. Bene, B. Pejcinovic and A. Baric, "Evaluation of the operation of depletion-mode SiC power JFET in DC-DC converter applications," in *Information and Communication Technology, Electronics and Microelectronics (MIPRO), 2014 37th International Convention on*, Opatija, 2014.
- [25] A. Anthon, Z. Zhang and M. Andersen, "A high power boost converter for PV Systems operating up to 300 kHz using SiC devices," in *Electronics and Application Conference and Exposition (PEAC), 2014 International*, Shanghai, 2014.
- [26] J. Hostetler, P. Alexandrov, X. Li, L. Fursin and A. Bhalla, "6.5 kV SiC normally-off JFETs - technology status," in *Wide Bandgap Power Devices and Applications (WiPDA), 2014 IEEE Workshop on*, Knoxville, TN, 2014.
- [27] F. Chevaliera, G. Grosseth, D. L., D. Tourniera, D. Planson and P. Brosselarda, "A path toward high voltage devices : 3.3 kV 4H-SiC JBS and JFET," in

HETECH 2012, Barcelone, 2012.

- [28] X. Song, A. G. Huang, C. Peng and L. Zhang, "Improved 6.5kV FREEMD-Pair based on SiC JFET and Si IGBT," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2016.
- [29] J. Biela, D. Aggeler, D. Bortis and J. W. Kolar, "Balancing circuit for a 5-kV/50-ns pulsed-power switch based on SiC-JFET super cascode," *IEEE Transactions on Plasma Science*, vol. 40, no. 10, pp. 2554-2560, 2012.
- [30] A. Daniel, C. Francisco, B. Juergen and W. K. Johann, "Dv/Dt-Control methods for the SiC JFET/Si MOSFET cascode," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 4074-4082, August 2013.
- [31] N. Oswald, P. Anthony, N. McNeill and B. Stark, "An experimental investigation of the tradeoff between switching losses and EMI generation with hard-switched All-Si, Si-SiC, and All-SiC device combinations," *Power Electronics, IEEE Transactions on*, vol. 29, no. 5, pp. 2393-2407, 1 May 2014.
- [32] D. Domes, C. Messelke and P. Kanschat, "1st Industrialized 1200V SiC JFET module for high energy efficiency application," Infineon Technologies AG., 2011.
- [33] R. Chacko, M. Ravichandran, M. Sanoop, T. Sabu, V. Sadasivan Achari and C. Joseph, "Magnetic slip ring rotary transformer based novel non-contact signal transfer mechanism for spacecraft application," in *Emerging Research Areas: Magnetism, Machines and Drives (AICERA/iCMMD), 2014 Annual International Conference on*, 2014.
- [34] R. Robutel, C. Martin, C. Buttay, H. Morel, P. Mattavelli, D. Boroyevich and R. Meuret, "Design and implementation of integrated common mode capacitors for SiC-JFET inverters," *Power Electronics, IEEE Transaction on*, vol. 29, no. 7, pp. 3525-3636, 2014.
- [35] K. Li, A. Videt and N. Idir, "Characterization method of SiC-JFET interelectrode capacitances in linear region," *IEEE Transaction on Power Electronics*, vol. 31, no. 2, pp. 1528-1540, February 2016.
- [36] S. Zeljkovic, R. Vuletic, A. Miller and A. Denais, "A three phase bidirectional V2G interface converter based on SiC JFETs," in *Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on*, Geneva, 2015.
- [37] S. Chen, J. He and K. Sheng, "High-voltage full-SiC power module: Device fabrication, testing and high frequency application in kW-level converter," in *Power Semiconductor Devices & IC's (ISPSD), 2015 IEEE 27th International Symposium on*, 2015.
- [38] A. Romani, A. Camarda, A. Baldazzi and M. Tartagni, "A micropower energy harvesting circuit with piezoelectric transformer-based ultra-low voltage start-up," in *Low Power Electronics and Design (ISLPED), 2015 IEEE/ACM International Symposium on*, Rome, 2015.
- [39] R. Jacek, P. Dimosthenis and N. Hans-Peter, "Design steps towards a 40-kVA SiC JFET inverter with natural-convection cooling and an efficiency exceeding 99.5%," *IEEE Transaction on Industry Applications*, vol. 49, no. 4, pp. 1589-1598, July-August 2013.
- [40] T. Friedli, S. D. Round, D. Hassler and J. W. Kolar, "Design and Performance of a 200-kHz All-SiC JFET Current DC-Link Back-to-Back Converter," *IEEE Transactions on Industry Applications*, vol. 45, no. 5, pp. 1868-1878, September/October 2009.
- [41] D. Pefitsis, G. Tolstoy, A. Antonopoulos, J. Rabkowski, J.-K. Lim, M. Bakowski, L. Angquist and H.-P. Nee, "High power modular multilevel converter with SiC JFETs," *IEEE Transaction on Power Electronics*, vol. 27, no. 1, pp. 28-36, 2012.
- [42] F. Xu, T. J. Han, D. Jiang, L. M. Tolbert, F. F. Wang, J. Nagashima, S. J. Kim, S. Kulkarni and F. Barlow, "Development of a SiC JFET-based six-pack power module for a fully integrated inverter," *IEEE Transaction on Power Electronics*, vol. 28, no. 3, pp. 1464-1478, 2013.
- [43] C. Buttay, D. Planson, B. Allard, D. Bergogne, P. Bevilacqua, C. Joubert, M. Lazar and C. Martin, "State of the art of high temperature power electronics," *Materials Science and Engineering: B*, vol. 176, no. 4, pp. 283-288, 2011.
- [44] W.-C. Lien, N. Damrongplisit, J. Paredes, D. Senesky, T.-J. Liu and A. Pisano, "4H-SiC N-Channel JFET for operation in high-temperature environments," *Electron Devices Society, IEEE Journal of the*, vol. 2, no. 6, pp. 164 - 167, November 2014.
- [45] D. J. Spry, P. G. Neudeck, L. Chen, D. Lukco, C. W. Chang and G. M. Beheim, "Prolong 500°C demonstration of 4H-SiC JFET ICs with two-level interconnect," *IEEE Electron Device Letter*, pp. 625-628, 2016.
- [46] P. G. Neudeck, D. J. Spry and L.-Y. Chen, "First-order SPICE modeling of extreme-temperature 4H-SiC JFET integrated circuit," 2016.
- [47] G. Tolstoy, A. K. Dutta and M. S. Islam, "Experimental durability testing of 4H SiC JFET integrated circuit technology at 727°C," in *Proc. SPIE 9836 Micro-and Nanotechnology Sensors, Systems, and Applications VIII*, Maltimore, Maryland, 2016.
- [48] A. Rahman, A. M. Francis, S. Ahmed, S. K. Akula, J. Holmes and A. Mantooth, "High-temperature voltage and current references in Silicon Carbide CMOS," *IEEE Transactions on Electron Devices*, vol. 63, no. 6, pp. 2455-2461, 2016.
- [49] D.-P. Sadik, J. Colmenares, D. Pefitsis, G. Tolstoy, J. Rabkowski and H.-P. Nee, "Analysis of short-circuit conditions for silicon carbide power transistors and suggestions for protection," in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, Lappeenranta, 2014.
- [50] G. Kampitsis, S. Papatthassiou and S. Manias, "Comparative evaluation of the short-circuit withstand capability of 1.2 kV Silicon Carbide (SiC) power transistors in real life applications," *Microelectronics Reliability*, vol. 55, no. 12, pp. 2640-2646, 2015.
- [51] X. Li, H. Zhang, P. Alexandrov and A. Bhalla, "Medium voltage power switch based on SiC JFET," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2016.

- [52] K. Y. J. Hsu and T.-W. Chuang, "An input buffer with monolithic JFET in standard BCD technology for sensor applications," in *Electron Devices and Solid-State Circuits (EDSSC), 2015 IEEE International Conference on*, Singapore, 2015.
- [53] Z. Miao, G. Sabui, A. Chen, Y. Li, Z. Shen, J. Wang, Z. Shuai, A. Luo, X. Yin and M. Jiang, "A self-powered ultra-fast dc solid state circuit breaker using a normally-on SiC JFET," in *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*, Charlotte, NC, 2015.
- [54] Z. J. Shen, G. Sabiu, M. Zhenyu and S. Zhikang, "Wide-bandgap solid-state circuit breakers for dc power systems: device and circuit considerations," *Electron Devices, IEEE Transaction on*, vol. 62, no. 2, pp. 294-300, February 2015.
- [55] V. Veliadis, B. Steinerb, K. Lawson, S. B. Bayne, D. Urciuo, H. Li and C. Ha, "Suitability of N-ON recessed implanted gate vertical-channel SiC JFETs for optically triggered 1200 V solid-state-circuit breaker," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. PP, no. 99, pp. 1-1, 2016.
- [56] M. Kemptkes, I. Roth and M. Gaudreau, "Solid-state circuit breaker for medium voltage dc power," in *Proceedings IEEE Electric Ship Technologies Symposium*, Alexandria, VA, 2011.
- [57] C. Meyer, S. Schroder and R. W. De Doncker, "Solid-state circuit breakers and current limiters for medium-voltage systems having distributed power systems," *IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1333-1340, September 2004.
- [58] D. P. Sadik et al, "Short-circuit protection circuits for Silicon Carbide power transistors," *IEEE transaction on Industrial Electronics*, vol. 63, no. 4, pp. 1995-2004, April 2016.
- [59] Z. Miao, G. Sabui, A. Maradkhani Roshandeh and Z. J. Shen, "Design and analysis of DC solid state circuit breakers using SiC JFET," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1-1, 2016.
- [60] X. Li, A. Bhalla, P. Alexandrov and L. Fursin, "Study of SiC vertical JFET behavior during unclamped inductive switching," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, Fort Worth, TX, 2014.
- [61] C. Sizhe, H. Junwei, W. Hengyu and S. Kuang, "Fabrication and testing of 3500V/15A SiC JFET based power module for high-voltage, high-frequency applications," in *Applied Power Electronics Conference and Exposition (APEC) 2015 IEEE*, Charlotte, NC, 2015.
- [62] A. Huang, X. Song and L. Zhang, "6.5 kV Si/SiC hybrid power module: An ideal next step?," in *Integrated Power Packaging (IWIPP), 2015 IEEE International Workshop on*, Chicago, IL, 2015.
- [63] D. Heer, R. Bayerer and D. Domes, "SiC-JFET in half-bridge configuration - parasitic turn-on at current commutation," in *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of*, Nuremberg, Germany, 2014.
- [64] P. Hazdra, S. Popelka, V. Zahlava and J. Vobecky, "Radiation damage in 4H-SiC and its effect on power electronic characteristics," *Solid State Phenomena*, vol. 242, pp. 421-426, 2016.
- [65] E. Velerander, A. Lofgren, K. Kretschmar and H.-P. Nee, "Novel solutions for suppressing parasitic turn-on behaviour on lateral vertical JFETs," in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, 2014.
- [66] X. Ni, R. Gao, X. Song, A. Huang and W. Yu, "Development of 6kV SiC hybrid power switch based on 1200V SiC JFET and MOSFET," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, 2015.
- [67] K. Okamura, K. Ise, M. Wake, Y. Osawa, K. Takaki and K. Takayama, "Characterization of SiC JFET in novel packaging for 1 MHz Operation," *Materials Science Forum*, Vols. 717-720, pp. 1029-1032, May 2012.
- [68] T. Singh and E. Kohn, "Harsh environment materials," in *Reference module in materials science and material engineering*, 2016.
- [69] S. Hazra, A. De, L. Cheng, J. Palmour, M. Schupbach, B. Hull, S. Allen and S. Bhattacharya, "High switching performance of 1700V, 50A SiC power MOSFET over Si IGBT/BiMOSFET for advanced power conversion applications," *Power Electronics, IEEE Transactions on*, vol. PP, no. 99, p. 1, 2015.
- [70] K. Chen, Z. Zhao, L. Yuan, T. Lu and F. He, "The Impact of Nonlinear Junction Capacitance on Switching Transient and Its Modeling for SiC MOSFET," *Electron Devices, IEEE Transactions on*, vol. 62, no. 2, pp. 333-338, February 2015.
- [71] J. Fabre, P. Ladoux and M. Piton, "Characterization and Implementation of Dual-SiC MOSFET Modules for Future Use in Traction Converters," *Power Electronics, IEEE Transactions on*, vol. 30, no. 8, pp. 4079-4090, August 2015.
- [72] K. Koiwa and J.-I. Itoh, "A Maximum Power Density Design Method for Nine Switches Matrix Converter Using SiC-MOSFET," *Power Electronics, IEEE Transactions on*, vol. 30, no. 2, pp. 1189-1202, February 2016.
- [73] X. Yang, B. Lee and V. Misra, "Investigation of Lanthanum Silicate conditions on 4H-SiC MOSFET characteristics," *Electron Devices, IEEE Transactions on*, vol. 62, no. 11, pp. 3781-3785, November 2015.



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