High Speed Level Converters With Short Circuit Current Reduction

Adipudi Bala Tripura Sundari and Avireni Srinivasulu, *SMIEEE*

***Abstract*—The level converter is used as interface between low voltages to high voltage boundary. The efficient level converter has less power consumption and less delay are the design considerations of the level shifter. In this paper two new CMOS level converters are presented with high driving capability and low propagation delay. The proposed level converters are simulated using Cadence software with 0.18 µm CMOS technology. The simulation result shows that the proposed circuits have less propagation delay than existing ones. The circuits are simulated with different load capacitor values and different voltages. The proposed level converters operate for different input pulse signal amplitude values are +0.8 V, +1 V, +1.2 V and V_{DDH} values of +1.8 V and +3.3 V.**

Keywords*— High speed, level converter, propagation delay, power converters, short circuit current

I. Introduction

Transistor sizes in CMOS process technology lead to many advantages in terms of speed and functionality of the level converter [1]-[11]. For maintaining reliability of system supply voltages come down when the size of the transistor is reduced. Level shifter is used in multi supply voltage systems where voltage difference problem exist. Level shifters are used in aero space systems, MEMS, power converters, and in microprocessors [12]-[21].

Conventional voltage level converter [2] is shown in Fig. 1. A low level voltage input signal V_i is applied to the transistor T_1 and complementary input signal is applied to the transistor T_2. The high level voltage output signals (V_{DDH}) are obtained at the node V_{op} and V_{on}. The input signal V_i is high transistor T_1 is ON and T_2 is OFF then the node V_{op} becomes High. V_{op} node decreases from High (V_{DDH}) to Low when the input signal changing from High (V_{DDH}) to Low. Transistor T_1 has to sink the load discharge current and extra short circuit current from T_3. The aspect ratios of PMOS transistors are larger than NMOS transistors because PMOS transistors have less transconductance. This requires large sized NMOS transistors to sink the PMOS current, it increases the short circuit currents. Short circuit currents increase the signal to noise ratio due to the impedance of supply rails.

Manuscript received July 6, 2014, revised September 22, 2014.

Adipudi Bala Tripura Sundari is with the Department of Electronics & Communication Engineering, VFSTR University (Vignan University), Vadlamudi-522213, Guntur, Andhra Pradesh, INDIA.

Avireni Srinivasulu is with the Department of Electronics & Communication Engineering, VFSTR University (Vignan University), Vadlamudi-522213, Guntur, Andhra Pradesh, INDIA. (Mobile: +91 9502223336; Fax No: +91 863 2534468; e-mail: avireni_s@yahoo.com (or) avireni@ieee.org).

The circuit presented in [3] is shown in Fig. 2. When the input V_i and output V_o both are low, then T_2 is ON. Input V_i goes high, transistor T_3 cannot OFF instantly, because its source is connected to the voltage V_{DDH} and gate terminal is connected to voltage V_{DDL}. As a result transistor T_1 sinks the short circuit current from the transistor T_3. Transistor T_2 acts as supply voltage switch for transistors T_3 and T_1. T_2 acts as high resistance switch, hence the input at the gate of T_2 increases slowly.

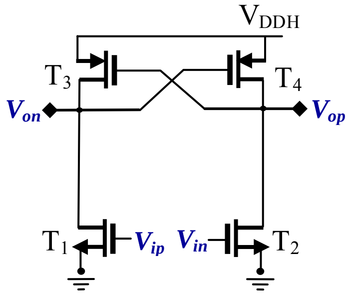

Fig. 1. Conventional voltage level converter [2].

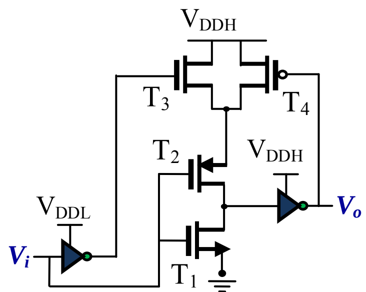

Fig. 2. Conventional voltage level converter [3].

A sub threshold to the above threshold level converter [4] is shown in Fig. 3. This circuit has two stages. First stage uses the cross coupled inverter configuration with NMOS diode connected transistor on top. Second stage is the DCVS logic inverter used for achieving full swing. This design is not useful for high speed, because the second stage of this design affected by short circuit current problem. Second stage of the circuit is DCVSL inverter, the gate of one pull up transistor (T_7) is connected to drain of another pull up transistor (T_8), so short circuit current flows in the circuit when the pull up transistors (T_7 and T_8) are OFF. So propagation delay is increased because the circuit pulls down slowly. The circuit in [4] has higher delay values for 500 mV. This circuit is not used for external loads because it is self loaded.

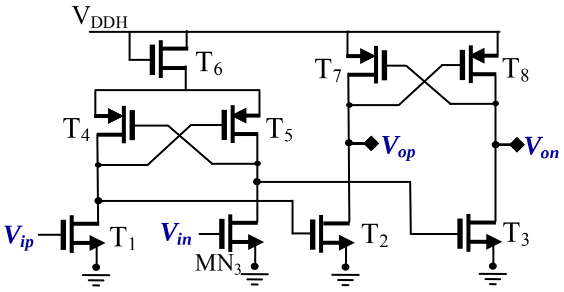

Fig. 3. Conventional voltage level converter [4].

Another Level converter presented in [5] is shown in Fig. 4. Its speed increased than [4] by inserting PMOS diode connected transistors. The diode connected transistors T_3 and T_4 are used to limit the leakage current from pull up transistors T_1 and T_2. This increases the speed of the circuit than Fig. 3. A voltage drop nearly equal to threshold voltage V_{th} occurs in PMOS transistor T_3 or T_4 helps to quickly turn ON the PMOS transistor T_1 or T_2 when these are OFF. The diode drop reduces the output swing; to increase the swing additional transistors T_5 and T_8 are added to pull down the output to low voltage level. The diode connected transistors are used to limit the short circuit current and to improve the speed performance. To reduce the short circuit current further an additional feature is added in [6] hybrid level converter.

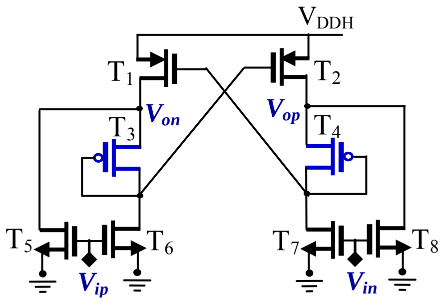

Fig. 4. Conventional diodes based voltage level converter [5].

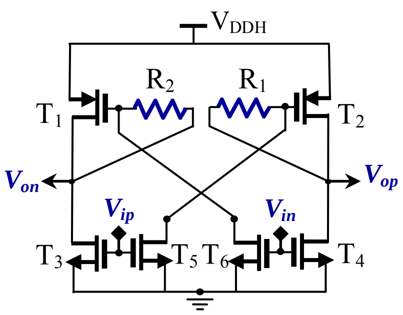

Fig. 5. Conventional voltage level converter with resistors to reduce short circuit current [6].

In Fig. 5 [6] a technique is introduced to reduce the short circuit current. In this technique the PMOS latch is modified by adding resistors R_1 and R_2. These resistances are replaced by NMOS transistors. Transistors T_5 and T_6 are used to minimize the short circuit current. Gate of each PMOS pull up transistor is separated by drain of other PMOS transistor with a resistance. The gate of PMOS transistor is pulled down by NMOS transistors T_5 and T_6 simultaneously. Resistors block the short current from transistors T_1 and T_2. Because of that PMOS transistors (T_1 and T_2) are pulled down quickly.

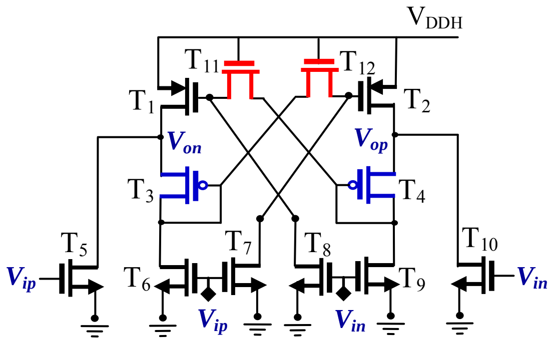

Fig. 6. Conventional hybrid voltage level converter [6].

For achieving high speeds high resistance is useful. When the resistance is high it perfectly blocks the short circuit current from transistors T_1 and T_2. The circuit presented in Fig. 6 [6] is implemented by combining resistive technique (Fig. 5) and diode technique (Fig. 4) in [5]. The final circuit implementation is shown in Fig. 6.

When V_{op} is high and V_{on} is low in Fig. 6 the gate of the transistor T_1 is high where as T_1 is completely OFF. Hence T_{11} has high resistance which helps to pull down the transistor T_1. The gate of T_2 is connected to ground so T_{12} has low resistance to pull up the transistor T_2. Then the output V_{op} become low and V_{on} become high. In this state the gate of the transistor T_2 is high when T_2 is completely OFF. Hence T_{12} has high resistance this is helped to pull down the transistor T_2. The gate of T_1 is connected to ground so T_{11} has low resistance to pull up the transistor T_2. Then V_{op} become high and V_{on} become low. Transistors T_9 and T_{10} are used to minimize the leakage current at pull up transistors T_1 and T_2.

II. PROPOSED LEVEL CONVERTER CIRCUITS

In the proposed circuits the resistors implemented by using NMOS transistors shown in Fig. 6 [6] are replaced by PMOS transistors and diode connected transistors are also replaced by PMOS transistors used as resistors to quickly pull up the transistors T_1 and T_2 in proposed voltage level converter circuit-I. To block the short circuit current two methods are preferred. One method is to increase the aspect ratios of NMOS transistors T_{11} and T_{12}. Due to the increased aspect ratios of the NMOS transistors area and power consumption of the level converter are increased. Another method is to use the PMOS transistors as resistors. Because PMOS transistors have higher resistance compared to NMOS transistors. The resistance must be high for achieving lesser delay values. If the resistance is high the short circuit flows into the pull up transistors is blocked before the gate terminal and that short circuit current is minimized through the transistors T_7 and T_8. The proposed level converter circuit-I is as shown in Fig. 7.

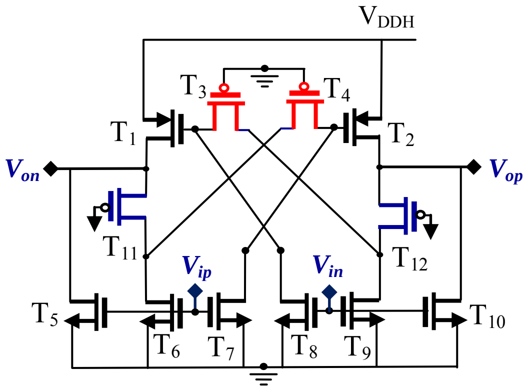

Fig. 7. Proposed voltage level converter-I.

When V_{op} is high and V_{on} is low in Fig. 7, the gate of the transistor T_1 is high whereas T_1 is completely OFF. Hence T_3 has high resistance this is helped to pull down the transistor T_1. The gate of T_2 is connected to ground so T_4 has low resistance to pull up the transistor T_2. Then the output V_{op} becomes low and V_{on} high. In this state the gate of the transistor T_2 is high, when T_2 is completely OFF. Hence T_4 has high resistance this is helped to pull down the transistor T_2. The gate of T_1 is connected to low voltage so T_3 has low resistance to pull up the transistor T_2. Then V_{op} become high and V_{on} become low. Transistors T_7 and T_8 are used to minimize the leakage current at pull up transistors T_1 and T_2. The input V_{ip} is high where transistor T_2 and T_7 are ON. The short circuit current flowing from the transistor T_2 is minimized through T_7. The input V_{ip} is low then transistor T_1 and T_8 are ON. The short circuit current flowing from the transistor T_1 is minimized through T_8. When the input voltage is in transition the operation of the circuit is explained in 3 regions.

Region 1: In region 1 the input V_{ip} is $0 \leq V_{ip} \leq V_{DDL}$ (where V_{DDL} is the HIGH logic level applied at the input of the level converter) T_1 is ON and T_2 is OFF and a short circuit current flows from the transistor T_2. Transistor T_3 blocks that short circuit current flowing from T_2. If a small amount of short circuit current crosses the transistor T_3 then that is grounded through the transistor T_8.

Region 2: In region 2 the input V_{ip} is equal to $V_{DDL}/2$ all the PMOS and NMOS transistors are ON. No short circuit current flows from the PMOS pull up transistors because both the pull up transistors ON. The node V_{op} raised from 0 to $V_{DDH}/2$ and the V_{on} falls from V_{DDH} to $V_{DDH}/2$.

Region 3: In region 3 the input V_{ip} is $V_{DDL}/2 \leq V_{ip} \leq V_{DDL}$ (where V_{DDL} is the HIGH logic level applied at the input of the level converter) T_2 is ON and T_1 is OFF and a short circuit current flows from the transistor T_1. Transistor T_4 blocks that short circuit current flowing from T_2. If a small amount of short circuit current crosses the transistor T_4 then that is grounded through the transistor T_9.

When short circuit current in the circuit is reduced the PMOS transistors quickly pulled down to LOW voltage level so response time of the output node V_{OP} is increased. So delay of the circuit is reduced.

T_{11} and T_{12} transistors are used as load helps to quickly turn ON the PMOS transistors. Transistors T_{11} and T_{12} are used to quickly pull up the output nodes V_{op} and V_{on} due to that raise time of the level converter is reduced. The proposed level converter circuit-II is as shown in Fig. 8.

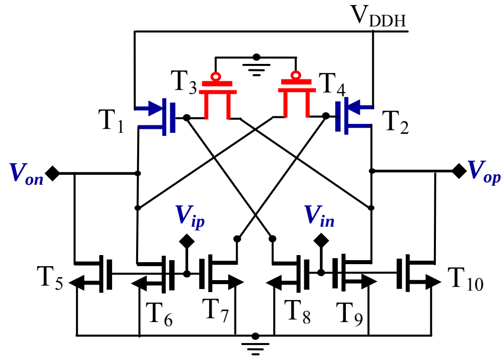

Fig. 8. Proposed voltage level converter-II.

When V_{op} is high and V_{on} is low in Fig. 8 the gate of the transistor T_1 is high so T_1 is completely OFF. Hence T_3 has high resistance which helps to pull down the transistor T_1. The gate of T_2 is connected to ground so T_4 has low resistance to pull up the transistor T_2. Then the output V_{op} become low and V_{on} become high. In this state the gate of the transistor T_2 is high so T_2 is completely OFF. Hence T_4 has high resistance which helps to pull down the transistor T_2. The gate of T_1 is connected to ground so that T_3 has low resistance to pull up the transistor T_2. Then V_{op} become high and V_{on} become low. Transistors T_7 and T_8 are used to minimize the leakage current at pull up transistors T_1 and T_2. When the input V_{ip} is high then transistor T_2 and T_7 are ON. The short circuit current flowing from the transistor T_2 is minimized through T_7. The input V_{ip} is low then transistor T_1 and T_8 are ON. The short circuit current flowing from the transistor T_1 is minimized through T_8. When the input signal is in transition the operation of the Fig. 8 is same as explained in the Fig. 7. T_5 and T_6 transistors are removed in Fig. 8 (proposed level converter circuit-II) to improve delay performance because a voltage drop V_{th} exists in T_5 and T_6 due to that the transistors T_1 and T_2 in Fig. 7 are not completely OFF, so delay of the circuit is increased. When the transistors T_{11} and T_{12} in Fig. 8 are removed T_1 and T_2 takes more time to pull up then raise time is slightly increased and fall time is reduced because no voltage drop exist in Fig. 8.

III. Simulation Results

The circuits are simulated for range of input pulse amplitudes of 0.8 V, 1 V and 1.2 V with the supply voltages of V_{DDH} = 1.8 V and 3.3 V using gpdk 180 nm CMOS technology at a frequency of 5 KHz.

TABLE I. PULSE INPUT PARAMETERS

S.No	voltage-1	0.8 V, 1 V, 1.2 V
1.	voltage-2	0 V
2.	delay time	2 ns
3.	raise time	1 ns
4.	fall time	1 ns

The simulated input and output waveforms for Fig. 7 are shown in Fig. 9 and Fig. 13. And the simulated input and output waveforms for Fig. 8 are shown in Fig. 10 and Fig. 14. The simulated DC responses for Fig.7 are shown in Fig. 11 and Fig. 15 and the simulated DC responses for Fig. 8 are shown in Fig. 12 and Fig. 16. The supply voltages are V_{DDH}=1.8 V, 3.3 V and input pulse amplitude of 1 V. Table-I represent the parameters of the pulse input applied at the input V_{ip} of the level converters. Table-II represents the aspect ratios of the transistors used in the implementation of proposed level converters.

TABLE II. ASPECT RATIOS

Transistor	Proposed level converter-I (Fig. 7)	Proposed level converter-II (Fig. 8)
	W (µm)/L (µm)	W (µm)/L (µm)
T_1,T_2,T_6,T_7,T_8,T_9	16/0.18	16/0.18
T_3,T_4	0.4/0.18	0.4/0.18
T_5,T_{10}	8/0.18	8/0.18
T_{11},T_{12}	40/0.18	-

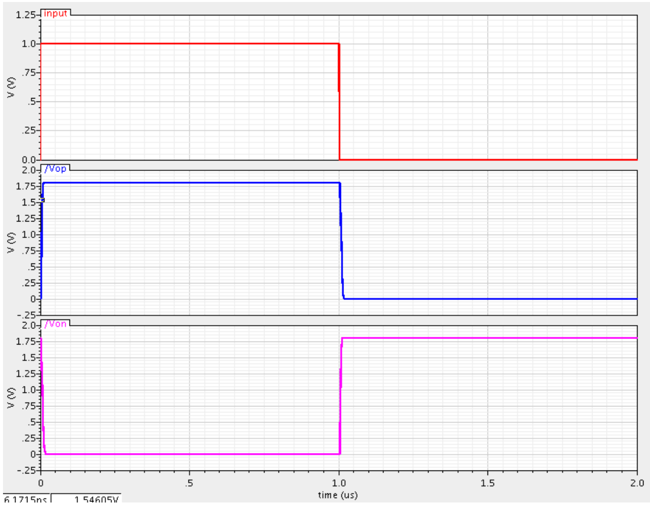

Fig. 9. Simulated input and output waveforms of Fig. 7 with load capacitance C_L=2 pF (Supply rail voltage V_{DDH}=1.8 V and input pulse amplitude=1 V).

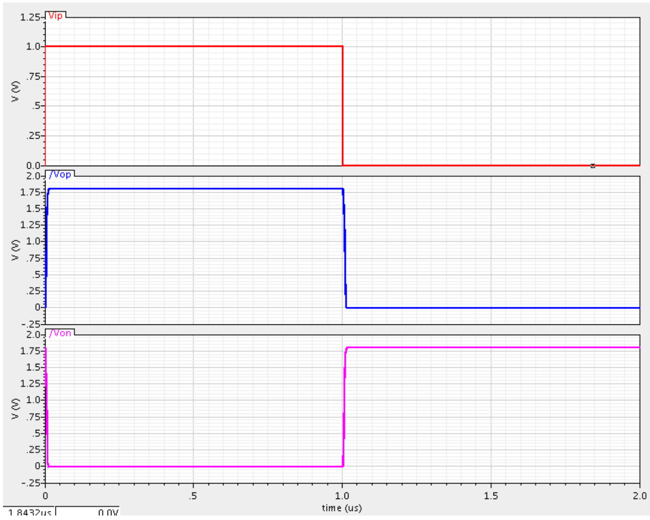

Fig. 10. Simulated input and output waveforms of Fig. 8 with load capacitance C_L=2 pF (Supply rail voltage V_{DDH}=1.8 V and input pulse amplitude=1 V).

Table III represents the comparison of simulated propagation delay values for proposed level converters with diodes based voltage level converter Fig. 4 and hybrid voltage level converter Fig. 6. In this table load capacitor values are varied from 2 pF to 25 pF, with input pulse amplitude of 1 V and frequency of 500 KHz. From table I it is clearly understand that there is a significant reduction of delay in the proposed level converters compared to existing circuits.

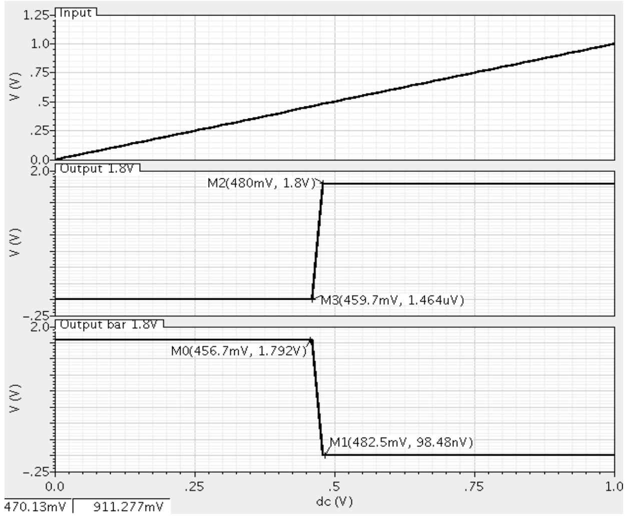

Fig. 11 Simulated DC response of Fig. 7 with load capacitance C_L=2 pF (Supply rail voltage V_{DDH}=1.8 V and input pulse amplitude=1 V).

Table IV represents the simulated values of propagation delay, raise time and fall time for Fig. 7 for different input pulse amplitude values (0.8 V, 1 V, and 1.2 V) and supply voltages V_{DDH} = 1.8 V and 3.3 V with different load capacitor values ranging from 5 pF to 15 pF. Table V represents the simulated values of propagation delay, raise time and fall time for Fig. 8 for different input pulse amplitude values (0.8 V, 1 V, and 1.2 V) and supply voltages V_{DDH} = 1.8 V and 3.3 V with different load capacitor values ranging from 5 pF to 15 pF.

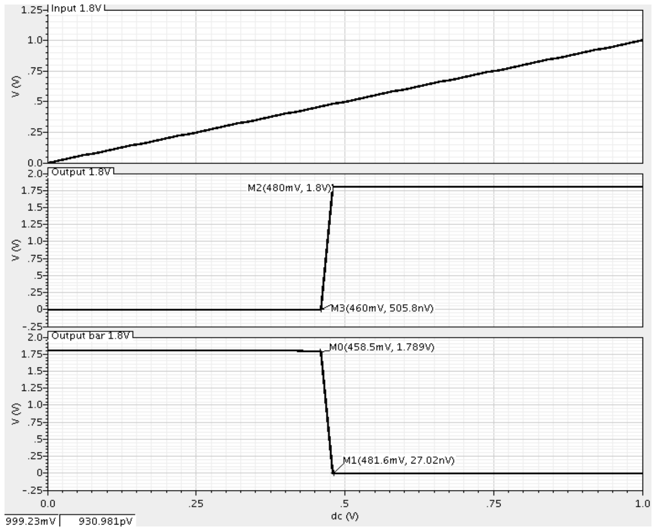

Fig. 12 Simulated DC response of Fig. 8 with load capacitance CL=2 pF (Supply rail voltage V_{DDH}=1.8 V and input pulse amplitude=1 V).

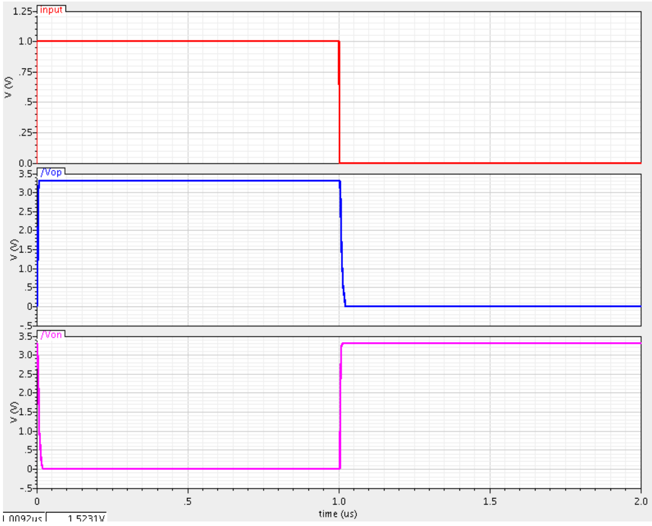

Fig. 13 Simulated input and output waveforms of Fig. 7 with load capacitance C_L=2 pF (Supply rail voltage V_{DDH}=3.3 V and input pulse amplitude=1 V).

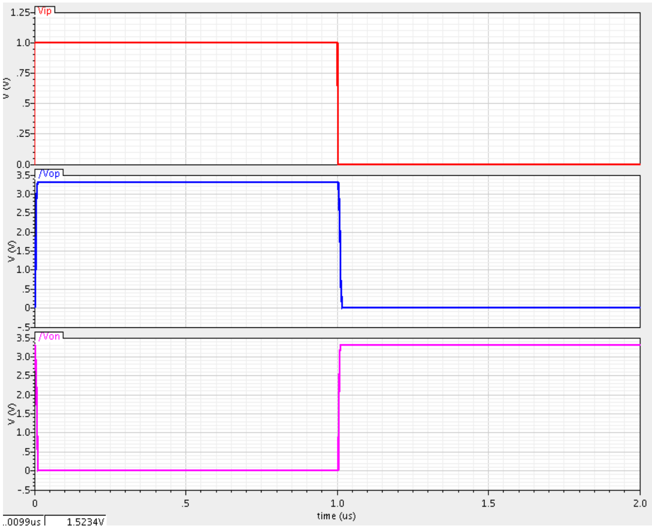

Fig. 14. Simulated input and output waveforms of Fig. 8 with load capacitance C_L=2 pF (Supply rail voltage V_{DDH}=3.3 V and input pulse amplitude=1 V).

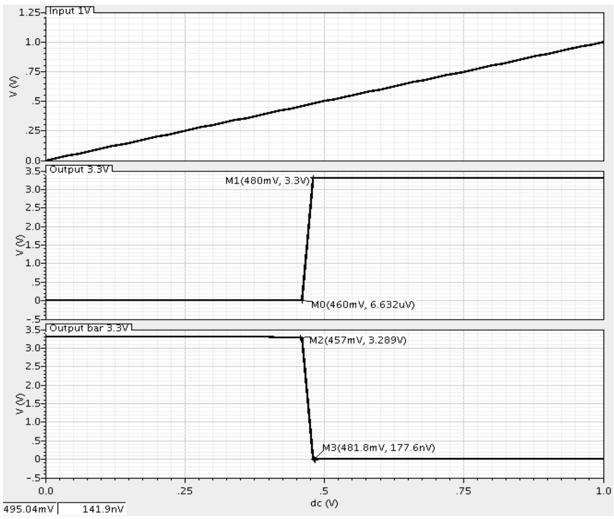

Fig. 15 Simulated DC response of Fig. 7 with load capacitance C_L=2 pF (Supply rail voltage V_{DDH}=3.3 V and input pulse amplitude=1 V).

Figure. 17 and 18 represents propagation delay comparison of proposed level converters and conventional level converters for different input pulse amplitudes ranging from 0.6 V to 1.4 V with supply voltages V_{DDH}=1.8 V and 3.3 V respectively. From Fig. 17 and 18 it is clearly understand that the proposed circuits have better speed performance than Fig. 4 and Fig. 6. When the input voltage amplitude is increasing speed performance of the circuit is increased. At lower supply voltages the speed of Fig. 4 and Fig. 6 is less compared with proposed circuits.

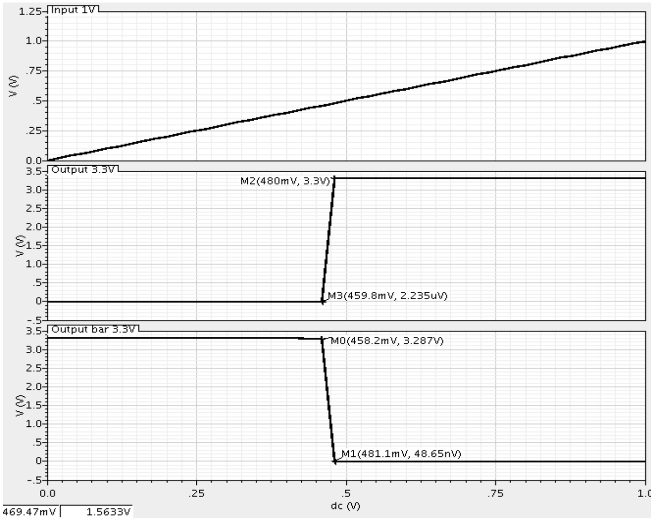

Fig. 16 Simulated DC response of Fig. 8 with load capacitance C_L=2 pF (Supply rail voltage V_{DDH}=3.3 V and input pulse amplitude=1 V).

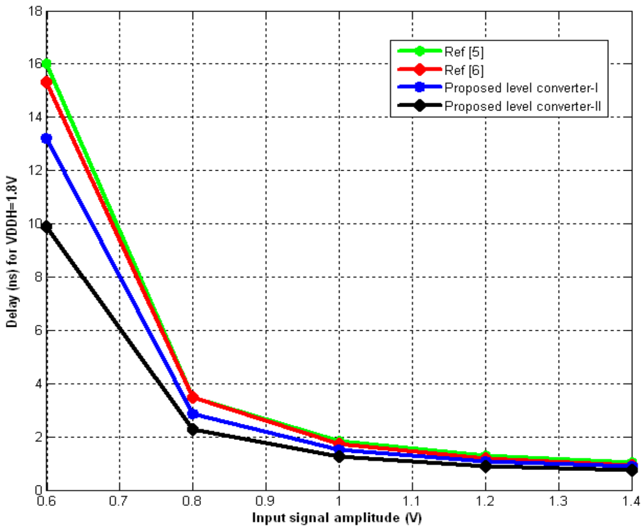

Fig. 17. Proposed level converters and conventional level converters propagation delay comparison for different input pulse amplitudes with supply voltage V_{DDH}=1.8 V.

Figure. 19 and 20 represents propagation delay comparison of proposed level converters and conventional level converters for different loading conditions with supply voltages V_{DDH}=1.8 V and 3.3 V respectively. When the load capacitor is increasing speed of the circuit is decreased. For V_{DDH} of 3.3 V Fig. 4 shows better performance than Fig. 6.

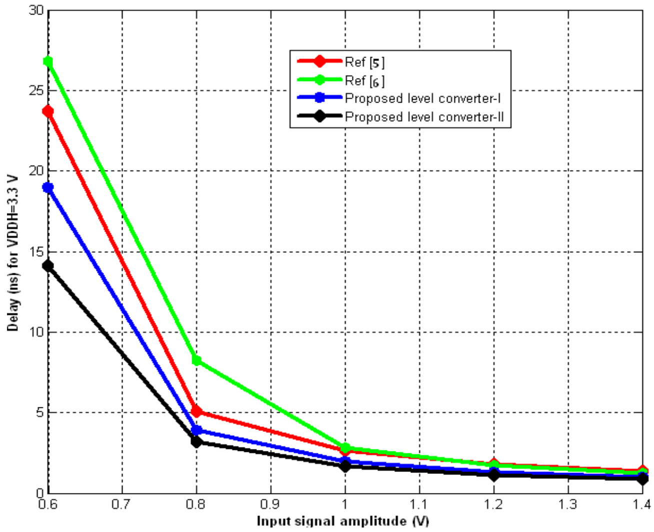

Fig. 18. Proposed level converters and conventional level converters propagation delay comparison for different input pulse amplitudes with supply voltage V_{DDH}=3.3 V.

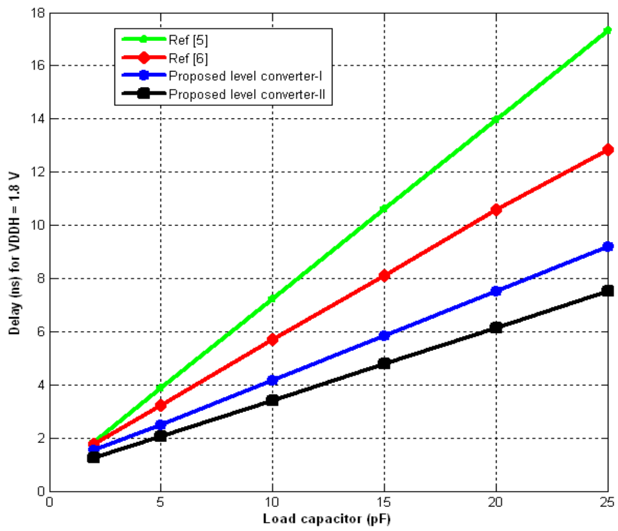

Fig. 19. Proposed level converters and conventional level converters propagation delay comparison for different loading conditions with supply voltage V_{DDH}=1.8V.

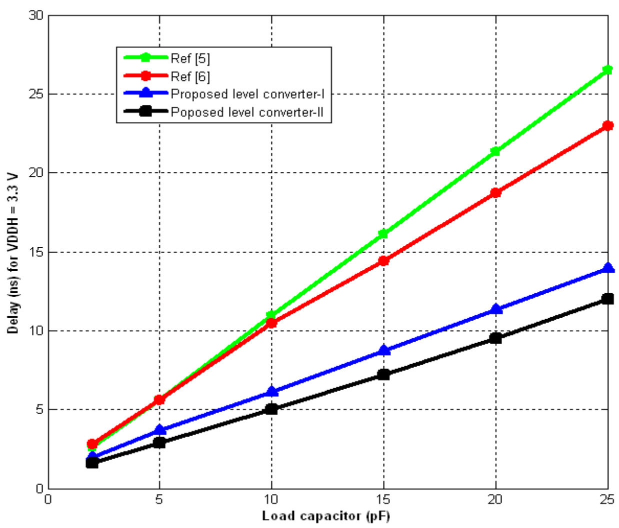

Fig. 20. Proposed level converters and conventional level converters propagation delay comparison for different loading conditions with supply voltage V_{DDH}=3.3 V.

Figure. 21 and 22 represents raise time comparison of proposed level converters and conventional level converters for different loading conditions with supply voltages V_{DDH}=1.8 V and 3.3 V respectively. From Fig. 21 and 22 it is clearly understand that proposed circuit Fig. 7 has less raise times than Fig. 4, 6 and 8. When the load capacitor is increasing raise time of the circuit is increased.

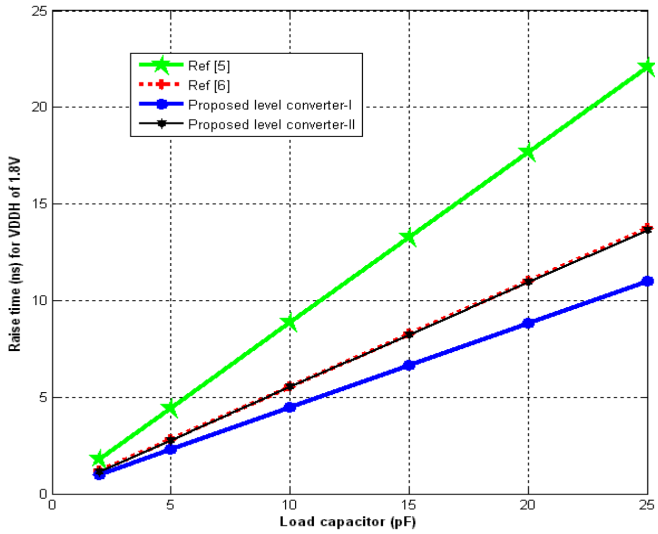

Fig. 21. Proposed level converters and conventional level converters raise time comparison for different loading conditions with supply voltage V_{DDH}=1.8 V.

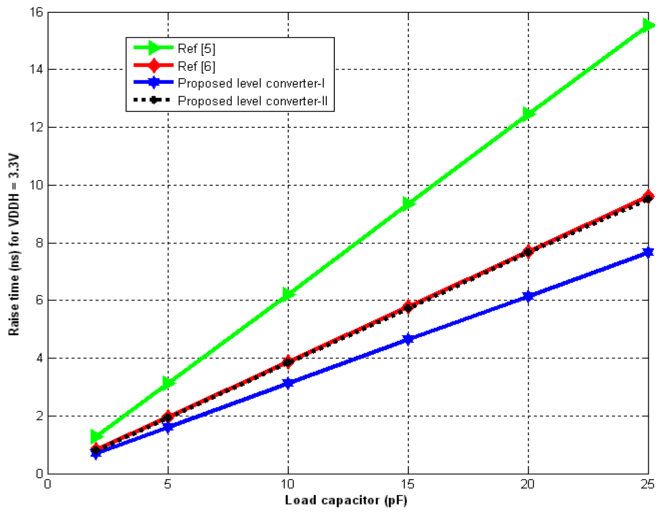

Fig. 22. Proposed level converters and conventional level converters raise time comparison for different loading conditions with supply voltage V_{DDH}=3.3V.

Figure 23 and 24 represents fall time comparison of proposed level converters and conventional level converters for different loading conditions with supply voltages V_{DDH}=1.8 V and 3.3 V respectively. From Fig. 23 and 24 it is clearly understand that proposed circuit Fig. 8 has less raise times than Fig. 4 and 6. When the load capacitor is increasing raise time of the circuit is increased.

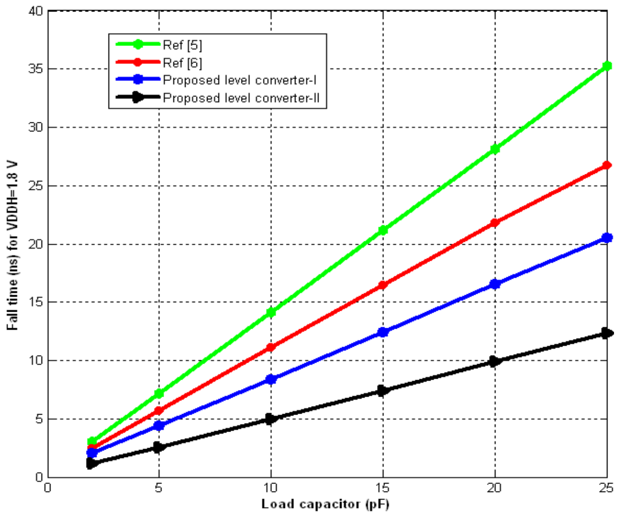

Fig. 23. Proposed level converters and conventional level converters fall time comparison for different loading conditions with V_{DDH}=1.8 V.

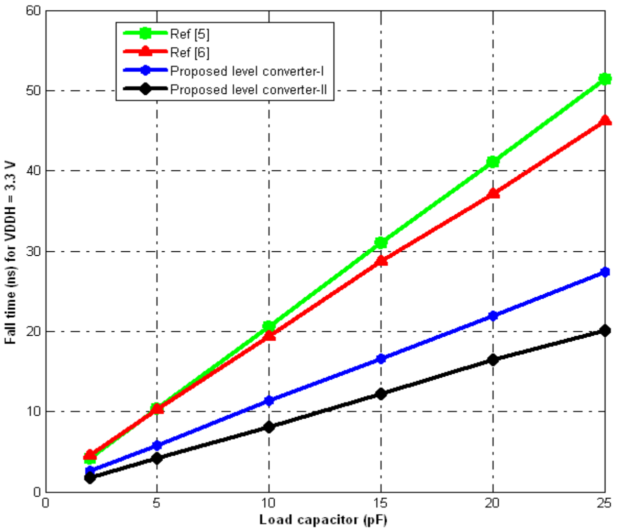

Fig. 24. Proposed level converters and conventional level converters fall time comparison for different loading conditions with supply voltage V_{DDH}=3.3V.

IV. Conclusion

Two Level converters with less delay are proposed using leakage current reduction technique. In leakage current reduction technique used in the existing circuit uses NMOS transistors as resistors by replacing NMOS transistors with PMOS transistors due to higher resistance of PMOS transistors speed performance of proposed circuits is improved. In the existing circuit's diode connected transistors drop a voltage V_{th}, by removing diode connected transistors speed performance of the circuit is further improved with small increase in raise time and decrease in fall time value in proposed level converter-II. Advantage of proposed level converter-I is it has less raise time.

References

[1] A.–J, Annema, B. Nauta, R. Van Langevelde and H. Tuinbout. "Analog circuits in ultra-deep-submicron CMOS", *IEEE Journal of Solid-States Circuits*, vol.40, no.1, DOI: JSSC.2004.837247, 2005, pp.132-143.

[2] D. Pan, Li, H. W. Wilamowski and B.M. "A low voltage to high voltage level shifter circuit For MEMS application", *in Proceedings of the 15th Biennial University/Government/Industry Microelectronics symposium*, DOI: UGIM.2003.1225712, 2003, pp. 128-131.

[3] Bo Zhang, Liping Liang, Xingiun Wang, "A new level shifter with low power in multi voltage system" *In proceedings of 8th International Conference on Solid-State and Integrated Circuit Technology*, DOI:ICSICT.2006.306488, 2006, pp.1857-1859.

[4] S.N. Wooters, B. H. Calhoun, T. N. Blalock, "An Energy-efficient sub threshold level converter in 130nm CMOS", *IEEE Transactions on circuits and systems-II Express Briefs*, Vol. 57, No. 4, DOI:TCSII.2010.2043471 April 2010, pp. 290-294.

[5] H. Shao, C. Y. Tsui. "A robust input voltage adaptive and low energy consumption level converter for sub-threshold logic", *in Proc. of 33rd European Solid-State Circuits Conf. (ESSCIRC)*, DOI:ESSCIRC.2007.4430306, 2007, pp.312-315.

[6] S. Ali, S. Tanner, P. A. Farine. "A robust, low power, high speed voltage level shifter with built-in short circuit current reduction", *in Proc. of 20th European Conf. on Circuit Theory and Design (ECCTD)*, DOI: ECCTD.2011.6043302, 2011, pp.142-145.

[7] I. J. Chang, J. -J. Kim, Roy and K. , "Robust Level Converter Design for Sub-threshold Logic", *in Proc. of the International Symposium on Low Power Electronics and Design (ISLPED)*, DOI:LPE.2006.4271800, 2006, pp.14-19.

[8] M. Vadipour, "A New compensation technique for resistive level shifters" *IEEE Journal of Solid-State Circuits*, vol.28, no.1, 1993, pp.93-95.

[9] Y.Kanno, H.Mizuno, K.Tanaka, T.Watanabe, "Level converters with high immunity to power supply bouncing for high speed sub 1v VLSIs" *In Proceedings of International Symposium on VLSI Circuits Digest of Technical papers*, DOI:VLSIC.2000.852890, 2000, pp.202-203.

[10] Wen-Tai Wang, Ming-Dou Ker, Mi-Chang Chiang, Chung-Hui Chen, "Level shifters for high speed 1V to 3.3V interfaces in a 0.13µm Cu-interconnection/low-k CMOS technology" *In Proceedings of International Symposium on Technical Papers*, DOI: VTSA.2001.934546, 2001, pp.307-310.

[11] Mahendranath. B and Avireni Srinivasulu, "Analysis of two new voltage level converters with various load conditions," International Journal of Advances in Telecommunications, Electrotechnics, Signals and Systems, vol. 2, no. 3, pp. 92-98, 2013. ISSN: 1805-5443.

[12] J.Kim, M. H. Kim, S.L. Kim, C. K. Jeon, Y. S. Choi, H. S. Kang, C. S. Song, "The new high voltage level up shifter for HVIC" *In proceedings of IEEE 33rd Annual Conference on Power Electronics Specialists*, vol.2, DOI: PSEC.2002.1022523, 2002, pp.626-630.

[13] C. Q. Tran, H. Kawaguchi, T. Sakurai, "Low power high speed level shifter design for block level dynamic voltage scaling environment" *In proceedings of International Conference on Integrated Circuit Design and Technology*, DOI:ICICDT.2005.1502637, 2005, pp.229-232.

[14] Won-Ki Park, Cheol-Ung Cha, Sung-Chul Lee, "A Novel level shifter circuit design for display panel drivers" *In Proceedings of 6th IEEE International Midwest Symposium on Circuits and Systems*, vol.2, DOI:MWSCAS.2006.382294, 2006, pp.391-394.

[15] J. F. da Rocha, M.B. dos Santos, J. M. Dores Costa, F. A. Lima, "Level shifter and DCVSL for a low voltage CMOS 4.2V buck converter" *IEEE Transactions on Industrial Electronics*, vol.55, no.9, DOI:TIE.2008.927974, 2008, pp.3315-3323.

[16] J. Rocha, M. Santos, J. M. D. Costa, F. Lima "High voltage tolerant level shifters and DCVSL in standard low voltage CMOS technologies" *In Proceedings of IEEE International Symposium on Industrial Electronics*, DOI: ISIE.2007.4374695, 2007, pp.775-780.

[17] J. C. Garcia, J. A. Montiel-Nelson, S. Nooshaadi, "High performance CMOS dual supply level shifter for a 0.5V input and 1V output in standard 1.2V 65nm technology process" *In proceedings of 9th International Symposium on Communications and Information Technology*, DOI: ISCIT. 2009. 5340988, 2009, pp.963-966.

[18] J. C. Garcia, J. A. Montiel-Nelson, S. Nooshabadi, "High performance bootstrapped CMOS dual supply level shifter for 0.5V input and 1V output" *In Proceedings of 12th Euromicro Conference on Digital System Design, Architectures, Methods and Tools*, DOI: DSD.2009.180, 2009, pp.311-314.

[19] Avireni Srinivasulu and M. Rajesh, "ULPD and CPTL pull-up stages for Differential Cascode Voltage Switch Logic," Journal of Engineering (*Hindawi*), vol. 2013, Article ID 595296, 5 pages, 2013. ISSN: 2314-4912.

[20] D. Wolpert, P. Ampadu, "Level shifter speed, power, and reliability trade-offs across normal and reverse temperature dependences" *In Proceedings of 53rd IEEE International Midwest Symposium on Circuits and Systems,* DOI: MWSCAS.2010.5548766, 2010, pp.1254-1257.

[21] Y. Moghe, T. Lehmann, T. Piessens, "Nanosecond delay floating high voltage level shifters in a 0.35µm HV-CMOS technology" *IEEE Journal of Solid-State Circuits*, vol. 46, no. 2, DOI: JSSC.2010.2091322, 2010, pp.485-497.

Adipudi Bala Tripura Sundari was born in Ongole, Prakasam District, (A.P), India in 1991. She received the B.Tech degree in electronics and communication engineering from J.N.T.University, Kakinada in 2012. She is now working towards her M.Tech thesis in VLSI Design at VFSTR University, Vadlamudi, Guntur, India. Her area of research includes VLSI Design and Microelectronics.

Avireni Srinivasulu was born in Thurimella, Andhra Pradesh, India. He received the B.Tech degree in electronics and communication engineering from Sri Venkateswara University, Tirupati in 1986, M.E, degree in power electronics engineering from Gulbarga University, Gulbarga in 1991, M.S, degree in software systems from Birla Institute of Technology and Science (BITS), Pilani in 1998 and Ph.D, degree in electronics and communication engineering (VLSI Design) from Birla Institute of Technology, Mesra, India in 2010. He is working as a Dean (R&D) and Professor of Electronics and Communication Engineering, VFSTR University, Guntur, India. He has 25 years of teaching and 15 years of research experience in the Department of Electronics and Communication Engineering.
Dr. Avireni.S is a senior member of IEEE, senior member of IACSIT, life member of I.S.T.E and a member of the Institution of Engineers (India). He has published over 50 articles in international journals and international conference proceedings; his main research areas are microelectronics, VLSI design and analog ASIC.

TABLE III. COMPARISON OF SIMULATED PROPAGATION DELAY VALUES OF PROPOSED LEVEL CONVERTERS WITH EXISTING LEVEL CONVERTERS IN DIFFERENT LOAD CONDITIONS.

Level converters	**Supply rail voltages**		**Propagation delay (ns)**					
	Input pulse amplitude (V)	**V_{DDH}**	**C_L= 2 pF**	**C_L =5 pF**	**C_L =10 pF**	**C_L =15 pF**	**C_L =20 pF**	**C_L =25 pF**
Fig. 4 [5]	1	1.8	1.853	3.865	7.229	10.604	13.97	17.33
Fig. 6 [6]	1	1.8	1.75	3.231	5.6895	8.12	10.571	12.84
Proposed level converter-I (Fig. 7)	1	1.8	1.551	2.483	4.154	5.837	7.53	9.216
Proposed level converter-II (Fig. 8)	1	1.8	1.254	2.047	3.4045	4.794	6.144	7.516
Fig. 4 [5]	1	3.3	2.65	5.595	10.95	16.12	21.34	26.537
Fig. 6 [6]	1	3.3	2.84	5.629	10.45	14.42	18.71	22.97
Proposed level converter-I (Fig. 7)	1	3.3	1.981	3.651	6.111	8.71	11.3	13.94
Proposed level converter-II (Fig. 8)	1	3.3	1.633	2.892	5.028	7.169	9.51	11.967

TABLE IV. COMPARISON OF SIMULATED PROPAGATION DELAY, RAISE TIME AND FALL TIME VALUES OF PROPOSED LEVEL CONVERTER-I (FIG. 7)

V_{DDH}	**Input pulse amplitude**	**Capacitor output load C_L**								
		5 pF			**10 pF**			**15 pF**		
		Raise time(ns)	Fall time(ns)	Propagation delay(ns)	Raise time(ns)	Fall time(ns)	Propagation delay(ns)	Raise time(ns)	Fall time(ns)	Propagation delay(ns)
1.8	0.8	2.327	9	4.893	4.51	17	8.338	6.69	24	11.79
1.8	1	2.3	4.74	2.483	4.47	8.548	4.154	6.645	12.54	5.837
1.8	1.2	2.3	3.413	1.9	4.471	5.947	3.005	6.645	8.577	4.122
3.3	0.8	1.6	11.74	7.203	3.124	22.66	12.66	4.643	33.67	18.18
3.3	1	1.503	5.88	3.651	3.115	11.19	6.111	4.631	16.56	8.71
3.3	1.2	1.59	4.082	2.427	3.113	7.533	4.039	4.63	11.09	5.68

TABLE V. COMPARISON OF SIMULATED PROPAGATION DELAY, RAISE TIME AND FALL TIME VALUES OF PROPOSED LEVEL CONVERTER-II (FIG. 8)

V_{DDH}	Input pulse amplitude	Capacitor output load C_L								
		5 pF			10 pF			15 pF		
		Raise time(ns)	Fall time(ns)	Propagation delay(ns)	Raise time(ns)	Fall time(ns)	Propagation delay(ns)	Raise time(ns)	Fall time(ns)	Propagation delay(ns)
1.8	0.8	2.784	5	3.84	5.505	11	6.46	8.216	16	9.093
1.8	1	2.784	2.597	2.047	5.505	4.967	3.4045	8.216	7.424	4.794
1.8	1.2	2.782	1.681	1.497	5.498	3.233	2.498	8.21	4.77	3.51
3.3	0.8	1.964	8.859	5.77	3.844	16.86	10.23	5.752	25.4	14.77
3.3	1	1.943	4.153	2.892	3.835	8.097	5.028	5.72	12.08	7.169
3.3	1.2	1.943	4.153	2	3.831	5.257	3.341	5.725	7.867	4.775